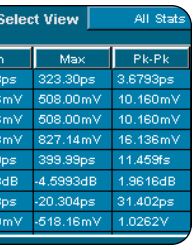
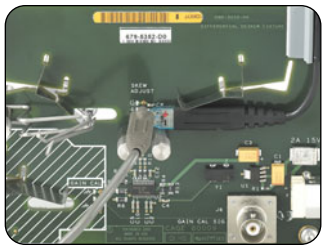
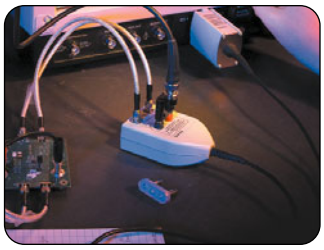
COMPUTING
COMMUNICATIONS
VIDEO

High-speed Differential Data Signaling and Measurements







Primer

Tektronix
Enabling Innovation

Part 1 – Differential Signaling

Part 2 – Differential Measurements

Part 1: Differential Signaling

Introduction

A significant transformation is taking place in data communication as digital interfaces are changing from wide bus structures to gigabit serial data links. Although there are a number of factors that are contributing to this change, the primary factor is the need to deal with increasingly difficult signal integrity issues as data rates continue to increase. Single-ended signaling with wide parallel buses appears to have finally reached its practical plateau in data rate and density. Differential signaling with gigabit serial data links is being selected as the technology for physical layer data transfer in many of the new data communication standards. The increased noise rejection and decreased noise generation, characteristic of differential signaling, have made possible this improved signal integrity performance. The application of differential signaling has also brought with it the need to understand differential measurement techniques. Tektronix is committed to providing the best differential measurement tools, including probing technology to make measurements in the most challenging applications. The first part of this two-part primer will examine the use of differential signaling in high-speed serial data links. The second part of the primer will review differential measurement techniques, with a special focus on the use of high bandwidth differential probes.

Data Communication Technology Transformation

The exponential growth in computing power, that has continued since the days of the first microprocessor, has driven a similar need for increased data communication transfer rate. For internal data communications between a computer and its memory or internal peripherals, a shared data bus has been the conventional interface structure. Internal communication data rates have been increased by increasing both the data clock rate and the width of the data bus. For external data communications between computers and local peripherals, a mix of high-speed parallel bus interfaces and low-speed serial data interfaces have been used. Because of the need to limit the size of interconnect cables, the bus width of external parallel bus interfaces has remained relatively narrow; performance has been improved in external parallel bus interfaces primarily by increasing data transfer rate. For external data communications between computers and remote peripherals or in a local area network, the need to transfer data over longer distances has required serial data interfaces. For these remote data communication applications, as well, the trend has been towards dramatically increased data rates to support network processing and storage.

Conventional Internal Data Bus Interface

An example of a conventional internal data bus structure is the PCI interface. The PCI bus is the high-performance successor to the original IBM PC internal peripheral bus, the ISA bus. With a clock rate of 33 MHz and a 32-bit data path width, the PCI bus provided more than an order of magnitude improvement in data transfer rate over the ISA bus when it was introduced in the early 1990s. Even with a 133 MB/s data rate, the PCI bus has continued to evolve to try to keep up with the data transfer needs of more powerful processors. Updates to the PCI standard have doubled both the clock rate to 66 MHz and the data path width to 64 bits. A more recent extension to the PCI standard, called PCI-X, has extended the performance up to another order of magnitude with multi-rate clocking and a more efficient data transfer protocol. Multi-rate clocking is a data transfer enhancement technique for synchronous clocked systems where two (DDR) or four (QDR) data transfers occur in each clock cycle. As the data rate has increased, the PCI standards have been forced to limit the number of bus loads and bus length to reduce signal integrity problems. The load limit in the PCI-X standard, for example, is only one bus load, with bus expansion requiring buffered bridge techniques.

Conventional External Data Bus Interface

An example of an external data bus structure for local peripherals is the SCSI interface. SCSI is a high-speed, daisy-chained cable interface for interconnecting a variety of peripheral devices using an intelligent protocol for data transfers. The original SCSI implementation, defined in 1986, provided an 8-bit wide, bi-directional data bus with a data transfer rate of 5 MB/s. Up to eight peripheral devices could be chained together over a 20-foot maximum cable length with resistive terminations required at each end of the bus. Although an optional 16-bit wide data bus version, Wide SCSI, was defined in the first major enhancement to the SCSI standard, performance improvements to SCSI have been primarily through a repeated doubling of the bus data rate. Increases in the SCSI data transfer rate have been limited not only by the maximum signaling speed possible from signal transceivers, but also by interconnect physics. Because of signal dispersion caused by electrical cable losses, which become worse at higher data rates, there is a tradeoff between data rate, cable length, and the number of device loads for single-ended SCSI signaling. Ultra SCSI, for example, provides for a 20 MHz data transfer rate, but reduces the maximum cable length to 10 feet for up to four device loads and only five feet for more than five device loads. The most recent enhancements to the SCSI interface have addressed these data rate and interconnect

limitations by introducing a low voltage differential (LVD) signaling specification. Because of the improved noise performance of differential signaling, SCSI LVD devices allow longer cable lengths to be used even in a bus interconnect environment.

Remote Data Communication Interface

An example of a remote data communication interface is Ethernet, which has been the dominant local area network standard since its introduction to industry in the early 1980s. Ethernet is a serial bus interface that initially provided a shared 10 Mb/s data rate between connected devices using a packet-based data transfer protocol. The initial version of Ethernet provided half duplex communication between devices connected together on a single shared transmission line. Ethernet handled the transmission contention problem between connected devices with a collision detection and retransmission protocol. Although the initial connection media used for Ethernet was coaxial cable, the use of less expensive twisted pair cable with phone jack connectors became dominant after the Ethernet 10Base-T standard was introduced in 1990. The first major improvement in Ethernet data transfer rate was a change from contention-based data transfers on a shared connection to switched data transfers on dedicated connections. Rapid increases in Ethernet data rates followed, first to 100 Mb/s with Fast Ethernet, then to 1000 Mb/s with Gigabit Ethernet (GBE), and most recently to 10 Gb/s with 10 Gigabit Ethernet (10GBE). At higher data rates Ethernet cabling distances are also limited by interconnect physics, but a variety of sophisticated physical layer implementations have been developed to overcome these limitations. An example is the multi-wire, multi-level logic technique defined for the 1000Base-T standard. The use of a sophisticated modulation technique, quality interconnect cable, and DSP processing has enabled the 1000Base-T standard to extend its maximum cable length to match the 100m distance limitation originally specified in the 10Base-T standard. At gigabit data rates the Ethernet physical layer implementation methods include optical interconnects as well as electrical interconnects. Although optical interconnects are more expensive than electrical interconnects, they have significantly better loss characteristics and will almost certainly become more common as data rates continue to increase.

Next Generation Data Bus Interface

In most of these data communication standard examples, the evolution towards faster and faster data rates was limited not only by current technology switching speeds, but also by signal integrity problems from using parallel busses and single-ended signaling. A practical limit appears to have been reached in the use of parallel, single-ended data transmission and a transformation is taking place to serial, differential data transmission. The parallel PCI bus, for example, may begin to be replaced within a few years by the high-speed serial bus called PCI Express. The PCI Express architecture uses low voltage, differential signaling, a packet-based data transmission protocol, and an extendable high-speed data rate beginning at 2.5 Gb/s. PCI Express uses a four-wire interface to provide a bi-directional transmit signal pair and receive signal pair on each serial data lane. It also defines the capability of aggregating lanes up to a width of 32 lanes, depending on the application. Although more wires are required per data bit than with a conventional data bus, the PCI Express message-based protocol and embedded clocking eliminates the need for the many data control signals required by a conventional data bus. The elimination of data transfer control signals in the PCI Express interface results in no major increase in the size of backplane connectors, even with four wires per bit for bi-directional differential signaling. The PCI Express data rate includes a 25% overhead for 8B/10B encoding. This data encoding provides a DC-balanced bit stream with high transition density and also provides special control characters for the data transfer protocol. The DC-balanced bit stream allows for AC-coupling and improved signal integrity, and the high transition density eases the task of clock recovery at the SERDES receiver.

(**NOTE:** A SERDES (serializer/deserializer) integrates the parallel-to-serial and serial-to-parallel functions into a common building block component for high-speed serial transmission.) The common mode noise rejection of the differential signaling used by PCI Express also allows a low-voltage swing that reduces the power requirements of signal drivers and reduces EMI problems.

The table below summarizes some of the differences between conventional and next-generation data transmission techniques:

Table 1. Comparison of High-speed Parallel and Serial Data Characteristics

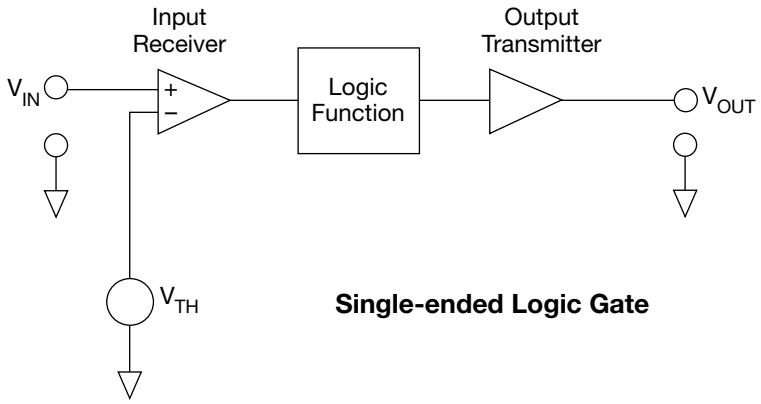
	Conventional Transmission	Next Generation Transmission
Signaling	Single-ended	Differential
Data Width	Parallel	Serial / Multi-lane
Interconnect	Shared Bus	Switched Point-to-Point
Transmission	Half Duplex	Dual Simplex
Clocking	Synchronous	Embedded
Data Transfer	Register-based	Message-Based
Data Element	Byte/Word	Data Packet
Data Control	Event Driven	Data Flow
Amplitude Limitation	Reflections, Crosstalk, and Noise	Loss and Dispersion
Timing Limitation	Skew	Jitter

One of the fundamental differences between conventional and next-generation data transmission is the type of signaling, which is changing from single-ended to differential. The next two sections of this primer will examine key differences between single-ended and differential signaling.

Single-ended Signal Transmission

The transfer of digital signals through a physical logic circuit requires an output transmitter and an input receiver at each stage of the transfer process. This is true, in general, whether the communication takes place between logic gates within an ASIC or across a back plane in a high-speed serial data link. A simple logic inverter, for example, can be considered to contain a single input receiver, a single output transmitter, and an internal logic inversion function. For lower speed logic, the interface between logic gates is usually shown as a single wire connection and the data transfer process can be referred to as single-ended signaling. This single wire connection, however, is in reality an abstraction, since any physical electrical signal requires a return current path. The return current path for single-ended logic signals is usually considered to be "ground," which is a common reference for all the logic devices on a circuit board or system. Even for single-ended data signals switching at very high speeds, where the interconnect between devices must be considered a transmission line, the signal return current path is still usually ground, implemented as a solid ground plane on a circuit board layer.

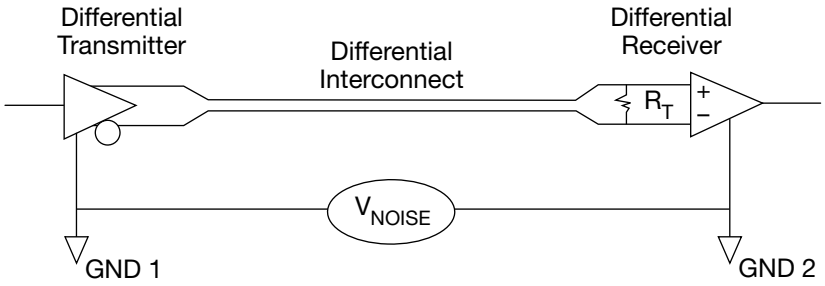
The common ground connection for single-ended signals provides not only a return current path, but also a stable voltage reference. Ground is generally used as the stable voltage reference for the internal logic threshold generator of each logic gate input. As shown in the block diagram in Figure 1, all single-ended logic gate inputs are in reality voltage comparators. The input to the gate is compared against an internal logic threshold voltage to determine whether the received input signal is a logic HI or logic LO. The threshold voltage generator in Figure 1 is shown referenced to ground, although, depending on the device family, the threshold generator may actually be referenced to the logic gate power supply. For TTL logic the input logic threshold voltage is established by the turn-on characteristics of several bipolar transistors that are connected together to form the TTL circuit topology. In the case of ECL logic the input structure is a bipolar transistor differential pair whose emitters are coupled to a common current source. When used for single-ended logic, an internal voltage generator in the ECL logic gate drives one side of the differential pair. This provides a comparator threshold voltage for the ECL input signal, which is connected to the other side of the differential pair. The input logic threshold of CMOS logic is established simply by the turn-on characteristics of the interconnected p-channel and n-channel MOS transistors in the CMOS circuit topology.



▶ ***Figure 1.*** *Single-ended signaling.*

Although single-ended logic families may generate their input logic threshold voltage in quite different ways, they all contain an embedded decision circuit. Even though single-ended logic gate inputs are shown schematically with only one input connection, there is actually an internal threshold comparison voltage that must be considered. The stability of this internal threshold voltage relative to the input signal swing can have a significant impact on the characteristics of the signal output from the logic gate. For example, noise sources that affect the input signal differently than the internal voltage threshold generator reference, can contribute to signal amplitude and timing distortion and even logic errors in the logic gate output. The switching of logic gate outputs, particularly devices with multiple outputs, can cause switching transients that effect the local ground potential, which then appears as noise injected into the internal threshold generator.

Single-ended signals are susceptible not only to switching noise on the ground reference, but also to interconnection noise problems. As system clock rates have increased above 100 MHz and signal density has increased beyond 32-bit bus widths, signal integrity issues have become more of a problem in the interconnection of single-ended logic signals. Signal reflections due to transmission line effects, and crosstalk between signals due to interconnect interaction, have all become increasingly troublesome as signal data rates and signal density have increased. Increased data rates and signal density have also created more of a problem with EMI, which has increased the expense of system shielding. The point has finally been reached where many digital communication designs are migrating from single-ended to differential signaling because of the improved signal integrity and reduced noise possible with differential signaling.



▶ ***Figure 2.*** *Differential signaling.*

Differential Signal Transmission

A differential signal is transmitted on a dual signal path and the two signals are driven as a complementary pair, with one signal the logical inverse of the other. As shown in Figure 2, differential signaling includes a differential transmitter, a differential interconnect, and a differential receiver.

Differential signaling is not new, but has been used for many years in long haul transmission applications, where the transmitter and receiver ground potential may be significantly different. In Figure 2, this ground potential difference between the transmitter and receiver is modeled as a noise voltage source and can have both DC and AC components. An example of the historical use of differential signaling techniques in a low-speed, analog application is the common telephone service, where a balanced voice signal is transmitted on a twisted pair transmission line to a balanced phone receiver. Differential signaling is used in local telephone service because of its noise rejection performance. The recent use of differential signaling in high-speed data links has occurred because of similar noise rejection advantages. High-speed data links, however, use differential signaling at much higher frequencies where noise problems tend to be more severe, even for relatively short connections.

The advantages of differential signaling in high-speed data transmission include the following:

- Common mode noise rejection
- Increased noise immunity
- Reduced crosstalk
- Reduced ground noise
- Reduced EMI

Differential signaling has much greater immunity to common mode noise problems than single-ended signaling because of both its interconnect topology and its signal processing technique. Differential signaling is able to reject common mode noise from ground potential variations between a transmitter and receiver, as well as crosstalk or other injected noise that is common to both signal paths. A differential signal interconnect is often routed as a coupled transmission line. This coupled transmission line topology provides a return current path between the coupled transmission lines, depending on the degree of coupling. For a balanced complementary signal transmitted on a tightly coupled transmission line, such as a twisted pair, the electric

fields are distributed primarily between the two signal conductors and the signal current propagating on one line returns on the other. The transmitted differential signal is then processed at the receiver as the voltage difference between the two lines. Differential signals thus carry along a built-in reference voltage that is largely independent of the ground potential at either the transmitter or the receiver. By processing the voltage difference between the two differential signals, the receiver effectively rejects most common mode noise that is present on both of the signals. By taking the difference between the two complementary signals, the differential receiver also produces twice the signal swing of a single-ended signal for improved noise immunity.

In addition to improved noise rejection, differential signaling also provides decreased noise generation, when compared to single-ended signaling. Crosstalk noise has become a major problem in dense, high-speed single-ended designs because of increased field coupling between closely spaced single-ended transmission lines. Since the field distribution in a tightly coupled transmission line driven by a complementary signal tends to be primarily contained between the two conductors, differential signaling generates less crosstalk than single-ended signals. Crosstalk reduction can also be helped by the fact that the two lines in a coupled line pair can be routed closer together, which should generally allow greater separation between groups of coupled pairs. The balanced nature of differential signals also generally leads to a more constant switching current than is seen with single-ended circuits. The signal currents in differential drivers tend to be steered between the two outputs as the signal polarity switches, which results in a more constant load current compared to the load current spikes commonly seen with single-ended drivers. Reduced load current transients should also result in a reduction of that portion of ground noise that is caused by current spikes passing through the ground lead inductance. This is particularly true of single-ended drivers for wide parallel bus registers where many bits may switch state simultaneously. The improved noise immunity and high sensitivity of differential receivers also allows the use of reduced logic swings with differential signaling. This smaller signal swing and the balanced field distribution associated with differential signaling also generate less EMI.

Although there are many advantages in using differential signaling, which has led to its increased use in high-speed data applications, the following disadvantages should be recognized:

- Increased layout complexity
- The need for balanced signals and interconnect

Routing two traces for every signal, of course, results in more complexity than routing only one trace per signal. In addition, the common use of point-to-point connections rather than a shared bus structure results in separate paths for transmit and receive signals, effectively doubling the number of signal pairs required in a high-speed serial link. Since the two traces of a differential signal are generally routed together as a coupled pair, this also adds to the complexity of the routing task. The routing of the traces in a differential signal must also be matched carefully in length and provide a symmetrical interconnect path and matched termination. Imbalance in differential signaling paths leads to the generation of common mode currents and reduced common mode rejection at the receiver.

Differential Signal Interconnects and Terminations

At gigabit serial data rates, differential signal interconnects must be handled as controlled impedance connections. A high-speed differential interconnect, whether within a cable or routed across a circuit board, should be designed with a characteristic impedance that ideally matches the output impedance of the transmitter driver. In addition, as shown in Figure 2, the differential signal transmission line should be terminated with a resistance that also matches the characteristic impedance of the interconnect. Finally, the differential signal interconnect should be routed with as short and clean a connection as possible to minimize parasitics that can lead to signal integrity and jitter problems with gigabit signals.

Differential Interconnects

Several high-speed serial data standards define an electrical cable interconnect in order to provide an extended range communication link between computing and data storage nodes. This electrical cable interconnect definition includes both circuit board mount connectors as well as transmission cable specifications. Most point-to-point serial data standards define independent differential signaling paths in each direction, both a transmit signal and a receive signal. This is generally referred to as a dual simplex communication link. This results in the typical pinout for a single lane connector having a four-wire signal interface and usually multiple ground pads. An electrical cable for the transmission of high-speed serial data will often be shielded and the differential signaling path will typically be implemented with twisted pairs. Twisted pairs are used for differential signal impedance control and to minimize crosstalk between the transmit and receive signaling pairs. Twisted pairs are a good example of tightly coupled transmission lines, which tend to pass differential mode signals and suppress common mode signals. Some serial data standards define multiple physical signaling lanes in a single communication port. InfiniBand, for example, defines 1X, 4X, and 12X signal lane connectors and cables.

High-speed serial data interconnects on circuit boards also require the use of differential signal routing techniques. At gigabit data rates differential signal interconnects are often routed as coupled transmission lines. Because of the generally close spacing between circuit board traces and board ground planes, the degree of coupling between differential lines on a circuit board is much less than for twisted pairs, particularly for edge-coupled lines. This limited coupling between circuit board differential pairs means that it is not uncommon to see differential pairs routed separately on circuit boards as two uncoupled transmission lines. This is especially true where differential pairs must be routed through connectors or other tightly spaced barriers that force the differential signals to be separated for some distance anyway. Even if a differential pair is routed as two uncoupled traces, however, they must still be carefully controlled for matched delay and routed as symmetrically as possible. Since routing a differential pair as a closely spaced, coupled line makes it somewhat easier to observe symmetry in routing, the use of coupled line routing is still very commonly used. Closely spaced differential pairs are somewhat less susceptible to crosstalk from adjacent signals, although the limited coupling between circuit board differential pairs means that crosstalk may be an important issue. Crosstalk will always be worse, of course, in densely routed circuit boards.

Coupling between the traces of a differential pair also results in a decrease in the differential mode characteristic impedance, which must also be taken into account in the layout design. This decrease in the differential mode characteristic impedance is the result of a decrease in the effective inductance and an increase in the effective capacitance of a coupled transmission line when driven with complementary signals. For a differential mode signal, the effective inductance of coupled transmission lines decreases due to the mutual inductance of the lines and the effective capitance increases due to the mutual capacitance of the lines. As the differential mode characteristic impedance decreases due to coupling effects, the common mode characteristic impedance, resulting from identical signal drive to each trace, increases. For the normal complementary signal drive applied to a differential signaling pair, common mode characteristic impedance is usually not a significant issue, since its effects are seen only with differential signal path imbalance, which should be minimized.

Coupled lines can be routed in several different ways, depending on the layout requirements. Edge-coupled lines, where the traces are routed side-by-side on the same circuit board layer, are commonly placed on the outer layers as microstrip lines, although they can also be embedded as inner layer striplines. Broadside-coupled lines, where the traces are routed on top of each other on different circuit board layers, should generally be routed only on inner layers as striplines in order to provide a symmetrical structure.

At gigabit data rates there are a number of high frequency effects that need to be considered with differential signal interconnects. As signaling frequency increases, electrical signals suffer increased attenuation due to skin effect and dielectric losses. In the case of cable interconnects this attenuation is usually characterized as insertion loss and pulse dispersion. For circuit board interconnects these same frequency dependent loss effects are seen, although the dielectric loss tends to dominate at multi-gigabit data rates particularly for the commonly used FR-4 circuit board material. Because of these loss effects, the trace length of differential signals should be minimized for high-speed data signals. Several of the high-speed serial data standards allow the use of pre-emphasis or equalization to try to compensate for these frequency dependent loss effects. Pre-emphasis (sometimes also called de-emphasis) is an increase in the transmitter drive signal in the first bit period following a change in signal polarity; the transmitter drive is then reduced in bit periods where there is no signal polarity change. Equalization is a high pass filtering technique applied to the signal interconnect to try to compensate for the increase in interconnect attenuation with frequency. The simplest implementation of equalization is the use of an AC-coupling capacitor, which forms a high pass filter with the termination resistor. Since the termination resistor value is set by the characteristic impedance of the interconnect, the value of the AC-coupling capacitor should be selected to match the desired equalization response.

There are also parasitic elements present in the interconnect paths of most differential signals that become more of a problem as gigabit data rates continue to increase. One example is the use of vias in the signal routing path, which sometimes must be used to move a signal from one circuit board layer to another. A via in the signal path introduces a parasitic capacitance and inductance that generally acts as a discontinuity in the transmission line, leading to possible reflection problems and perhaps some slowing of the signal edge. A through-hole via may also introduce a short stub, if the signal is transferred between other than the outer layers. Blind or buried vias can be used to minimize via parasitics, but generally at an increased circuit board cost. If vias must be used in the signal routing path, via design should try to minimize parasitics and the parasitics should be matched in both traces of a differential pair. Electromagnetic modeling tools are now readily available for use in extracting via parasitics and other high frequency parasitic effects. Other examples of routing path parasitics are the parasitic input capacitance present at the input pin of a serial data receiver and the package parasitics present in a circuit board mounted serial data connector.

Differential Terminations

Properly matched source and load terminations can minimize the effect of interconnect parasitics by absorbing the reflections from parasitic discontinuities. Differential signal transmission lines should be terminated with a resistance that matches the characteristic impedance of the lines. Depending on the requirements of the differential driver and receiver circuits, this termination may be either a single resistor, which terminates only the differential mode impedance of the coupled line, or a multiple resistor network to terminate both the differential mode and common mode impedances of the differential pair. The more complex multiple resistor termination network may also include some common mode capacitance and the insertion of a DC bias. In the case of some serial data transceivers, these termination resistors are internal to the transceiver in order to minimize package parasitics and also to simplify the interconnection task. The termination resistor network is sometimes also affected by whether the differential signal path is AC or DC coupled, with AC coupling often used for DC-balanced protocols, like those with 8B/10B encoding.

Many of the new serial data communication standards implement the physical layer interconnect with SERDES devices or circuits. A SERDES provides the interface between a byte-wide data stream and a high-speed serial data stream and may contain encoding, synchronizing, and clock recovery circuitry. The high-speed serial output of some SERDES devices is implemented with current mode logic (CML). CML was originally a variant on a bipolar ECL output structure, where the output emitter followers were removed. CML can also be implemented, however, with MOSFET transistors, with the transistors configured as a steered current source switch. A CML output structure is a switched current source output topology that is usually loaded with an internal 50 Ω pull-up resistor on each line of the output pair. These CML output pull-up resistors serve as a source termination or back termination for the transmission line interconnect. The CML transmission line interconnect should, of course, also be terminated at the receiver end of the line. This use of both source and load terminations on the transmission line interconnect provides an ideal signal path for high-speed serial data signals and is being commonly used now, especially for multi-gigabit data signals.

Physical Layer Standards for Serial Data Communication

A number of high-speed serial data communication standards have been introduced recently to address the need for next generation I/O connectivity. Some examples of these new interface standards are

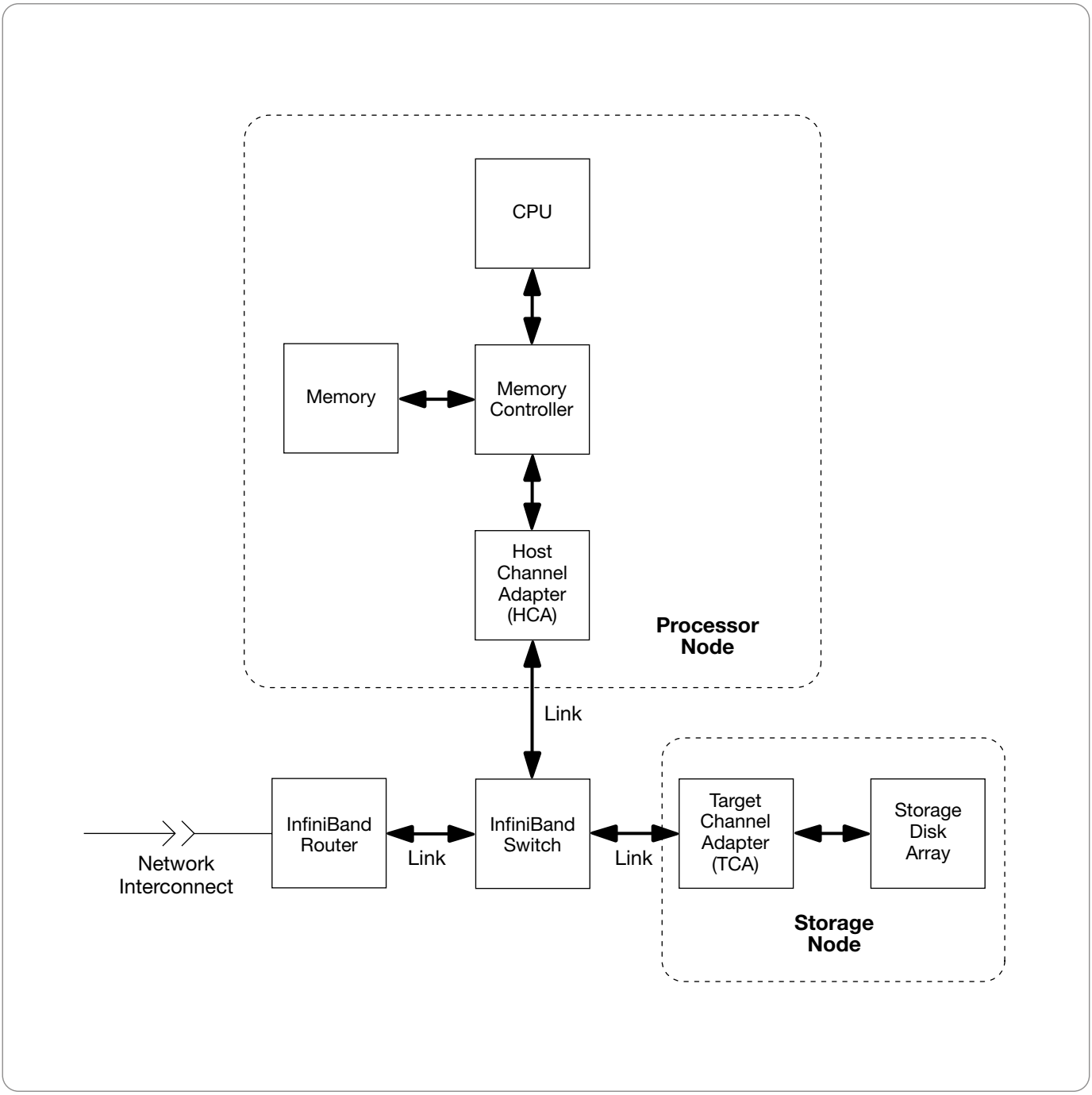
- InfiniBand
- PCI Express
- Serial ATA
- XAUI

Each of these standards shares a common 8B/10B encoding scheme and uses a similar differential signaling transmission topology, even though each was developed for a somewhat different application. InfiniBand was developed for use in the Internet data center to provide an improved data communication interface between compute servers, high-speed storage arrays, and Internet access devices. PCI Express was developed as a replacement for the PCI interface in high performance applications and was designed to be backward compatible with PCI at the software level. Serial ATA is a high-speed serial replacement for the parallel ATA interface (also called an IDE interface) used on many PC disk drives. XAUI is a 4-lane, chip-to-chip interface intended to provide a reliable connection between the system electronics and optical transceiver in a 10 Gigabit Ethernet interface.

Although each of these standards has some similar features, the underlying communication protocols and specification details differ significantly between the standards. Even the signaling rates are somewhat different, reflecting different applications and requirements. Although the signaling rate for InfiniBand and PCI Express is the same at 2.5 Gb/s, the signaling rate for Serial ATA is only 1.5 Gb/s, while the rate for XAUI is 3.125 Gb/s. In the case of XAUI, the use of 4 lanes each operating at 3.125 Gb/s results in the 12.5 Gb/s signaling rate required to give a 10 Gb/s data rate plus 25% overhead for 8B/10B encoding. The InfiniBand standard will now be examined in more detail, as an example of one of the new high-speed serial data communication standards.

InfiniBand

InfiniBand was developed as a next generation communication interface and is intended to be much more than just a local processor bus interface replacement. InfiniBand is designed for application flexibility over a variety of physical media. It is specified for use over short distances (<20 in.) as a processor backplane interface. It is also specified for use over extended distances (<17 m) as an electrical cable interface. It can even be used over longer distances as an optical cable interface, either with short wavelength fiber for distances of 75 m and more or with long wavelength fiber for a distance of up to 10 km. InfiniBand was designed to overcome the communication performance bottleneck in the Internet data center by addressing the limitations of a hierarchical, memory-mapped tree structure protocol like PCI. InfiniBand was designed as an intelligent I/O interface that would relieve compute servers, storage servers, and Internet routers of some of the processing overhead currently required to support I/O transfers.



▶ ***Figure 3.*** *The InfiniBand architecture.*

As shown in Figure 3, the InfiniBand architecture includes a

- Host Channel Adapter (HCA)
- Target Channel Adapter (TCA)
- InfiniBand Switch
- InfiniBand Router

The HCA is intended to reside in a compute server and manage its communication interface. The TCA is intended to reside in a storage array and provide an intelligent interface to a physical disk drive. The InfiniBand Switch is a fully mapped switch interface between multiple HCAs and TCAs in a local communication network. The InfiniBand Router is designed as an interconnection between local networks using existing network protocols, such as IPv6. For high performance at the protocol level, the InfiniBand architecture provides peer-to-peer communication through device channels rather than hierarchical communication from a memory-mapped

The InfiniBand Electrical Signaling specifications are defined in detail in Chapter 6 of Volume 2 of the InfiniBand Architecture specification. Table 2 highlights the key electrical specifications, which will be examined in more detail in the section that follows.

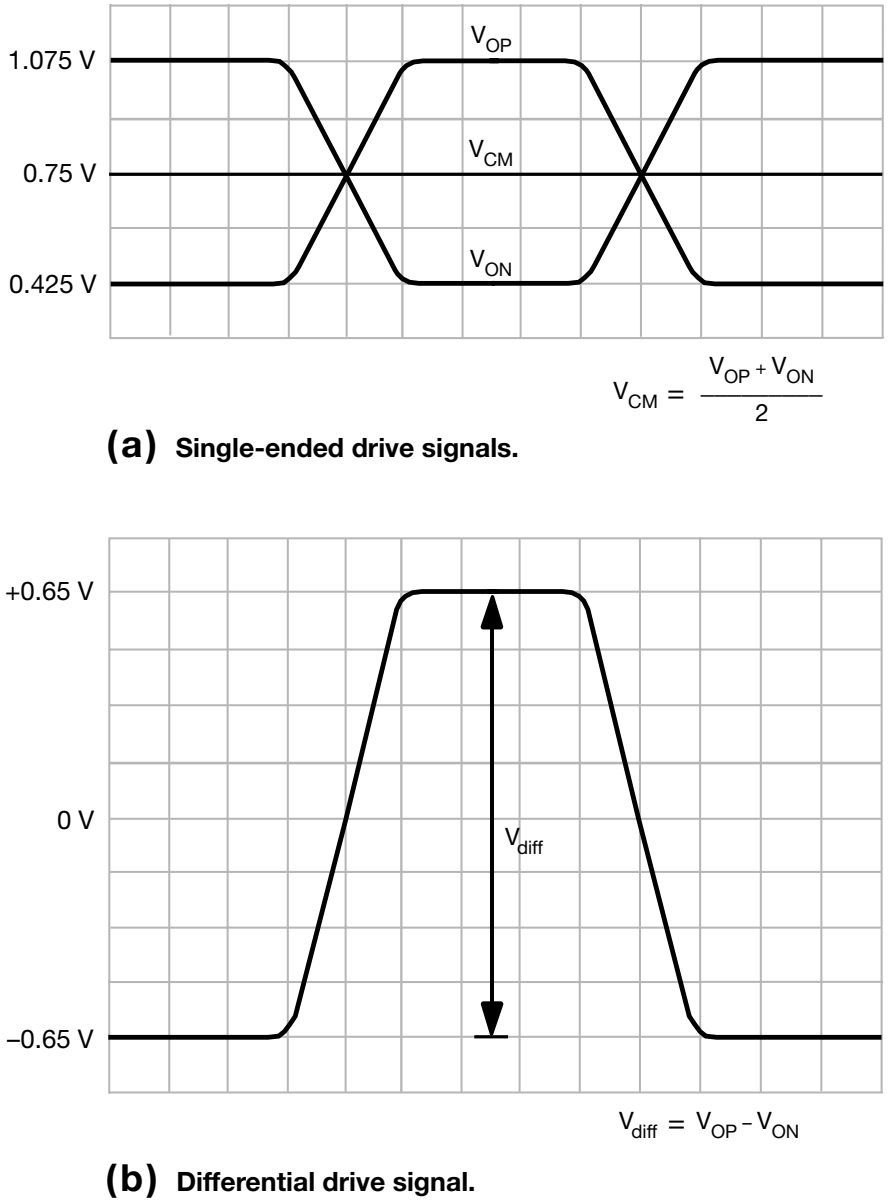
Table 2. InfiniBand Electrical Signaling Specifications (partial list from Release 1.1)

Impedance					
Driver	Symbol	Parameter	Max	Min	Units
	Z_D	Differential Output Impedance	125	75	Ω
	Z_{SE}	Single Ended Output Impedance	75	30	Ω
	Z_{MSE}	Single Ended Impedance Match	10		%
Receiver					
	Z_{RTerm}	Termination	62.5	40	Ω
	L_{DR}	Differential Return Loss		10	dB
	L_{CMR}	Common Mode Return Loss		6	dB
Amplitude					
Driver	Symbol	Parameter	Max	Min	Units
	V_{diff}	Differential Output (pp)	1.6	1.0	V
	V_{CM}	Common Mode Voltage	1.0	0.5	V
	$V_{disable}$	Disabled Mode Output	1.6	1.0	V
Receiver					
	V_{RSense}	Input Sensitivity (pp)		175	mV
	V_{RCM}	Common Mode Voltage	1.25	0.25	V
	V_{tt}	Termination Voltage	1.0	0.5	V
Timing					
Driver	Symbol	Parameter	Max	Min	Units
	UI	Unit Interval	400	400	ps
	t_{DRF}	Driver Rise/Fall Time		100	ps
	J_{T1}	Total Jitter at Driver	.35		UI
Receiver					
	t_{REye}	Eye Opening		140	ps
	J_{TR}	Total Jitter at Receiver	.65		UI
	S_{RBtB}	Total Skew	24		ns

central control processor. InfiniBand data transfer protocols support prioritization of data packets that, at the high InfiniBand transfer rate, enables the transfer of real time data with guaranteed quality of service. The InfiniBand protocols also support more reliable data communication through the use of error checking codes embedded in InfiniBand data packets.

At the physical layer, InfiniBand provides improved performance through its point-to-point, serial data interface. An InfiniBand communication lane includes two independent differential signaling paths, one for transmit and one for receive, both operating at a 2.5 Gb/s rate. The InfiniBand standard also includes scalable performance through the use of multiple lane links, with 1X, 4X, and 12X links currently specified. As a server backplane interface, the InfiniBand interface is hot-pluggable, which allows for ease of use in scaling compute power in servers and is beneficial for maintenance of a reliable server system. As a cabled interconnect interface between compute servers or storage arrays, the InfiniBand interface has been optimized for low-power operation by limiting the electrical cable length to 17 m, sufficient for the intended application in an Internet data center.

The InfiniBand impedance specifications define the limits for the InfiniBand signal interconnect environment. Since the InfiniBand differential signaling interconnect is designed for a nominal 100 Ω differential impedance, it might seem unusual for the driver impedance parameters, Z_D, Z_{SE}, and Z_{RTerm} to have such loose tolerances. Although the loose impedance tolerance specified will result in poorer



▶ ***Figure 4.*** *InfiniBand driver signals: V_{CM} = 0.75 V; V_{diff} = 1.3 V.*

signal integrity under worst-case conditions, it provides compatibility with integrated circuit processes. The use of integrated driver source resistance and receiver termination resistance, in turn, will actually help signal integrity because of the reduced termination parasitics. The single-ended impedance matching parameter, Z_{MSE}, is also compatible with integrated circuit processes and such matching is necessary to minimize differential signal imbalance. Differential signal imbalance causes some of the differential mode signal to be converted to a common mode signal, which can result in possible signal integrity or EMI problems. The receiver termination parameter, Z_{RTerm}, is a single-ended impedance value and the differential termination impedance is of course double that value.

The receiver return loss parameters, L_{DR} and L_{CMR}, are intended to guarantee a clean transmission line environment into the receiver. Differential and common mode return loss measurements, however, require a network analyzer with a mixed mode S-parameter test set and mixed mode conversion software. Most of the impedance parameters are specified over a bandwidth of 100 MHz to 1.875 GHz, a frequency range that includes most of the signal power spectrum for an 8B/10B encoded InfiniBand signal at 2.5 Gb/s.

The InfiniBand amplitude specifications define the allowable range of signal voltage between the driver and receiver. Since InfiniBand uses differential signaling, both differential mode and common mode parameters are specified. The common mode parameters are significant only for DC-coupled interconnections. The InfiniBand standard requires that cable connections be AC-coupled and allows backplane connections to be optionally AC-coupled. The standard also suggests a minimum DC blocking capacitance of 4700 pF, which gives a coupling impedance of much less than 1 Ω at 250 MHz. The 250 MHz frequency is noted here, since it is the lowest signaling frequency for an 8B/10B encoded signal with a 2.5 Gb/s signaling rate. This is the result of the 5-bit run length limit that is characteristic of 8B/10B encoding. The driver differential output parameter is specified for backplane interconnects at the output pins of the driver and will be attenuated due to interconnect losses if measured further down the interconnect path. If a backplane driver uses pre-emphasis, the differential output parameter range applies only to the first bit period following a transition and may be lower for later bits after the pre-emphasis drive is removed. For cable interconnects the differential output parameter is specified at the cable port and its range is valid with or without pre-emphasis. As shown in the Figure 4 example, the differential output parameter is specified as a peak-to-peak voltage difference, thus the signal swing on each pin of the driver is half that value. It should be noted that the V_{diff} parameter signal shown in Figure 4(b) can only be measured with a differential probe connected between the two signals in Figure 4(a), or by calculating the waveform difference of the two signals in Figure 4(a), measured with single-ended probes. The signal shown in Figure 4(b) thus represents the result of the receiver processing of the two complementary input signals from the driver shown in Figure 4(a) and cannot be measured directly as a single-ended signal. When the transmitter driver is in a disabled mode state, the differential output voltage is allowed to drop to zero volts, although the driver pins should still be held within the common mode voltage range. When the transmitter is in disabled mode and no differential voltage is applied to the receiver, the receiver must also be disabled to guarantee no false signals are generated. The input sensitivity parameter of an InfiniBand receiver is the minimum peak-to-peak differential signal that will be properly detected with the specified maximum bit error rate of 1×10^{-12}. Detection of signals below the input sensitivity level is not guaranteed. The receiver termination voltage range and common mode voltage range are only applicable for DC-coupled interconnects to the driver.

The InfiniBand timing specifications are designed to guarantee that the critical jitter characteristics of a high-speed serial link are controlled for reliable link performance. The InfiniBand timing parameters are based on eye pattern measurements*[1]. A unit interval (UI) of an eye pattern is the time window of a single bit period, which for 2.5 Gb/s signaling is 400 ps. The jitter on a signal can be observed at the transition edges on an eye pattern. The total jitter at the driver, which includes both random and deterministic jitter components, is specified for an InfiniBand backplane interconnect at a little over one-third of a UI. The total jitter spec for a cabled interconnect, although not included in the partial specification table, is more restrictive than for a backplane interconnect to allow more margin for jitter accumulation in a long cable interconnect. The difference between the total jitter allowed at the transmitter and the larger total jitter allowed at the receiver is an indication of the jitter that is allowed to accumulate over the length of the interconnect. The receiver eye opening parameter is a measure of the jitter-free time period in the center of the eye pattern at the receiver, and when combined with the receiver input sensitivity parameter can be used to define an eye pattern mask for signal transmission within allowable error limits. There are now more sophisticated jitter analysis tools, such as TDSJIT3 or TDSRT-Eye™ to use with real-time Tektronix oscilloscopes. These tools enable a more detailed analysis of the different jitter components.

*[1] An eye pattern is an overlapped display of signals showing the accumulation of all signal states in a single bit period window. It is called an eye pattern because of its eye shaped display and because the characteristic closing of the eye pattern as attenuation and jitter increase with interconnect length, causing the signal to no longer be "visible" to the receiver. Eye pattern jitter parameters are specified in terms of a unit interval.

The driver rise and fall time parameters are specified as minimum values to control signal integrity problems that become worse with faster edge speeds. The driver maximum rise/fall time, although not directly specified, is effectively controlled by the receiver eye opening mask, since too slow a transition at the transmitter will continue to slow through the interconnect and will cause mask violations at the receiver. It should be noted that the driver rise/fall time is specified as a 20-80% measurement, rather than the 10-90% measurement commonly used to specify the performance of measurement instruments. Since rise/fall times occur at signal transitions, if pre-emphasis is used in a driver, the rise/fall time measurement is made on the signal with pre-emphasis applied. The total skew parameter at the receiver may seem to be extremely large, since it equals 6 UI, but it represents skew across physical lanes of an InfiniBand port and can be compensated as part of the data synchronization and alignment process in the InfiniBand training protocol. The skew allowed between lanes driven from a single transmitter driver is much less (500 ps) and the skew between lines of a single lane differential pair, although not directly specified, should be kept as small as possible to ensure transmitting a good signal and to reduce signal integrity and EMI problems.

Part 1 Summary

This brief review of key critical signal parameters that must be measured to guarantee compliance with the InfiniBand physical layer standard is typical of the measurement requirements for new high-speed serial data communication standards. The standard tool used to make most of the voltage and timing measurements discussed in the last section is a high performance oscilloscope. Although at one time the high bandwidth necessary to measure gigabit data signals required the use of sampling oscilloscopes, dramatic improvements in real time oscilloscope performance have now made the use of real time oscilloscopes common in serial data measurements. Although an oscilloscope is a common measurement tool for testing standards compliance and debugging electronic circuitry, its use in making differential signaling measurements is perhaps less familiar. The focus of Part 2 of this primer will be on differential measurements, with an emphasis on their application to high-speed serial data communication signals.

Part 2: Differential Measurements

Introduction

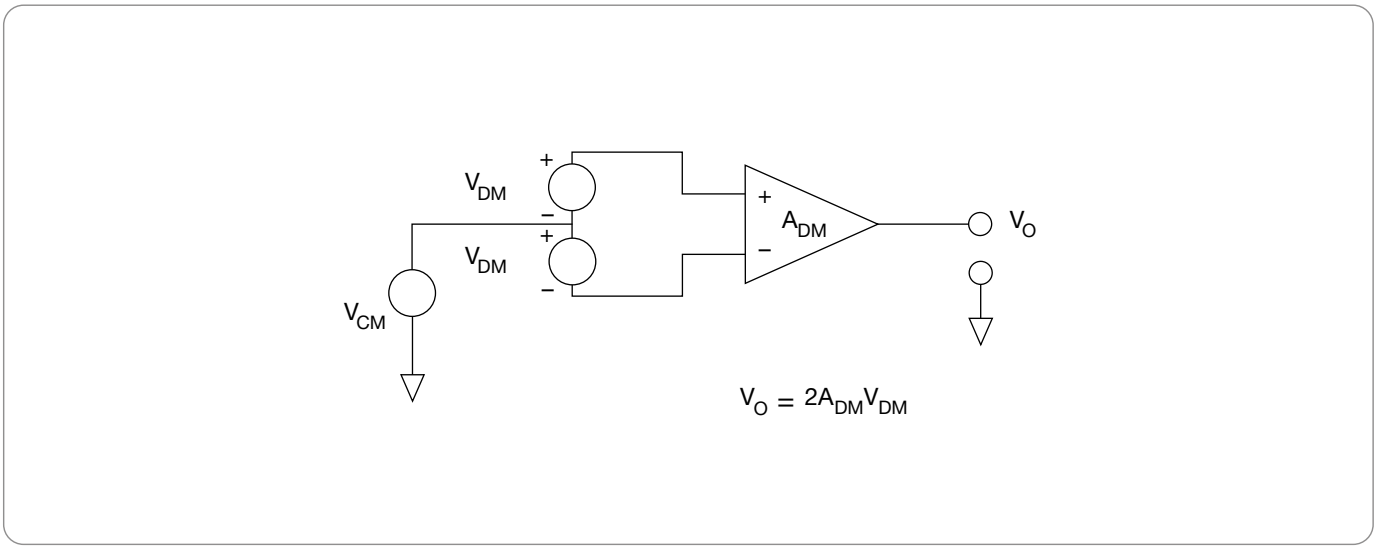
Part 1 of this primer discussed how the transformation led from single-ended signaling to differential signaling in new interface standards. It reviewed key differences between single-ended and differential signaling and the advantages of using differential signaling in high-speed data links. The application of differential signaling has also brought with it the need to understand differential measurement techniques. Because two single-ended signals are combined to make one differential signal, differential signaling adds complexity to signal characterization. Differential signaling generally requires that both differential mode and common mode parameters be specified. Similarly, differential measurements must deal with measuring both the differential mode and common mode parameters that describe the differential signaling interface. Part 2 of this primer will review differential measurements and the tools used to measure differential signals. Because of their importance in measurement fidelity, high-performance differential probes will be examined in considerable detail.

Differential Measurement Fundamentals

Although single-ended measurement tools can be used to indirectly measure differential signals, the use of differential measurement tools allows a designer to see the differential signal in much the way a differential receiver sees it. A good differential measurement tool must have the following characteristics to be able to measure a high-speed differential signal with good signal fidelity:

- ▶ High frequency response
- ▶ High common mode rejection
- ▶ High sensitivity and response accuracy
- ▶ Low noise floor
- ▶ Light circuit loading (unless designed to be a broadband termination)

An idealized differential amplifier is shown in Figure 5 driven by a combination of differential and common mode voltage sources. The voltage sources in Figure 5 are configured to model a complementary differential signal. The differential amplifier in Figure 5 might be considered to represent an ideal differential probe model, with infinite input impedance, a fixed differential mode gain, infinite CMRR, and an ideal 50 Ω output impedance to drive a probe cable.



▶ ***Figure 5.*** *Ideal differential amplifier.*

An ideal differential amplifier amplifies the voltage difference between its inputs, totally rejecting any voltage common to both inputs. Referring to Figure 5, the voltage, V+, on the differential amplifier positive input is

$$V_+ = V_{CM} + V_{DM}$$

The voltage, V–, on the differential amplifier negative input is

$$V_- = V_{CM} - V_{DM}$$

The resulting difference voltage output from the differential amplifier with fixed differential mode gain, A_{DM}, is

$$V_O = A_{DM} * (V_+ - V_-)$$

$$V_O = A_{DM} * [(V_{CM} + V_{DM}) - (V_{CM} - V_{DM})]$$

$$V_O = A_{DM} * (2\ V_{DM})$$

This resulting output voltage shows the rejection of the common mode input voltage and the doubling of the single-ended, differential mode input voltage.

The previous differential input equations show that the common mode voltage represents the average of the voltage on the two differential inputs

$$V_{CM} = (V_+ + V_-) / 2$$

Similarly, the differential voltage output from a unity gain differential amplifier is simply the voltage difference between the two differential inputs

$$V_{DIFF} = V_+ - V_-$$

A non-ideal differential amplifier will have slight imbalances between its two inputs, which results in a small portion of the common mode input voltage being passed through to the output. This common mode voltage signal in the output can be considered to be an undesirable error term, since part of it may result from ground noise or other common mode noise sources. Since it is possible to measure the response of a non-ideal differential amplifier to a purely common mode input signal, the common mode gain for the amplifier can be calculated:

$$A_{CM} = V_O / V_{CM} \quad \text{with } V_{DM} = 0$$

A measure of the performance of a differential amplifier in rejecting the undesirable common mode input signal is called the common mode rejection ratio (CMRR)

$$CMRR = A_{DM} / A_{CM}$$

Since the CMRR of a quality differential amplifier is a very large value, it is often expressed in decibels

$$CMRR = 20 \log (A_{DM} / A_{CM}) \text{ in dB}$$

As an example of the magnitude of the common mode error term in a good quality differential amplifier, consider an amplifier with a DC CMRR of 60 dB and a 1 V DC common mode input signal. Since a 60 dB CMRR is a 1000:1 gain ratio, the resulting DC error from the 1 V common mode input is 1 mV. The polarity of the 1 mV error term is unknown, since the CMRR measurement contains no phase information. Since common mode signals will, in general, have both AC and DC components, the CMRR frequency response of the differential amplifier must be considered. The CMRR of a typical

differential amplifier is generally highest at DC and drops off with increasing frequency, becoming significantly worse at high frequencies. This decrease in CMRR with frequency is a measure of the difficulty in maintaining balanced amplifier response as high frequency parasitic effects increase.

Differential Probe Specifications

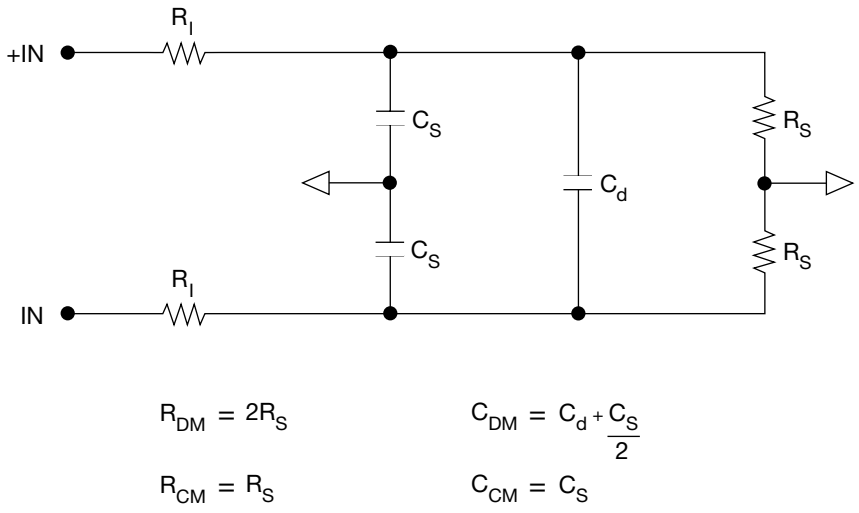
An oscilloscope specifies its measurement performance at its front panel input connector. The purpose of an oscilloscope probe is to extend specified measurement performance from an oscilloscope front panel to the circuit-under-test with the highest possible signal fidelity. Making high-fidelity measurements with a probe a meter or two away from an oscilloscope requires that the probe be connected to the oscilloscope with a high frequency, shielded cable. Since the coaxial cables commonly used to make this connection have a characteristic impedance of 50 Ω and a distributed capacitive load of about 30 pF/ft., a probe design must compensate for this cable loading. Passive probes, which connect to a high impedance, 1 MΩ oscilloscope input, compensate for cable loading by using a high impedance probe tip attenuator. The high impedance 10X attenuator commonly used in passive probes generally limits probe bandwidth to 500 MHz or less. For higher frequency applications, active probes are generally used.

Although an ideal differential probe would be able to measure a signal with perfect fidelity and without any loading of the signal, any real probe has limitations that must be understood. By understanding the limitations of practical probe performance, a user can more readily relate measured signal response to real signal response. By choosing a probe and scope whose performance is adequate for the measurement application and using the probe in a manner which minimizes its limitations, a user will get the best match between measured and real signal performance. The limitations of probe response are quantified with the probe performance specifications. Table 3 lists some of the key performance specifications for the Tektronix P7350, which is a high performance differential probe designed for use in applications like high-speed serial data signal analysis. The definition of the P7350 specifications listed in Table 3 will be examined in some detail in the following section. It should be noted that Table 3 contains a mix of guaranteed and typical specifications. The P7350 probe data sheet or User Manual should be consulted for more detail about a specific parameter.

Table 3. P7350 Electrical Characteristics

Parameter	Specification	Notes
Input Loading		
Differential Mode Input Resistance	100 kΩ ±2%	
Common Mode Input Resistance	50 kΩ ±2%	per side
Differential Mode Input Capacitance	<0.3 pF	at 100 MHz
Common Mode Input Capacitance	<0.45 pF	per side at 100 MHz
Amplitude Response		
DC Gain Accuracy	0.16 ±2%	6.25x attenuation
Differential Mode Input Range	±2.5 V	differential offset = 0
Common Mode Input Range	+6.25 V to –5.0 V	
Maximum Input (non-destructive)	±15 V	
Differential Offset Range	±1.25 V	
CMRR	DC 1 MHz 30 MHz 1 GHz	>60 dB >55 dB >50 dB >30 dB
Timing Response		
Bandwidth	DC to 5 GHz	3 dB bandwidth
Rise Time	<100 ps <65 ps	10 to 90% rise time 20 to 80% rise time

Active probes, which are designed to connect to a broadband, 50 Ω oscilloscope input, compensate for cable loading by using a high frequency buffer amplifier in the probe tip. The buffer amplifier in an active probe tip has a 50 Ω output driver stage that drives the distributed probe cable loading as a transmission line. Driving the probe cable as a transmission line provides broadband frequency response. The probe cable, however, like all transmission lines is susceptible to electrical cable loss. To guarantee signal fidelity, the probe buffer amplifier must compensate for probe cable frequency dependent loss effects, up to the frequency limit of the probe. The use of a high-frequency buffer amplifier in the probe head also reduces probe loading effects at the probe tip. The addition of a high impedance attenuator in front of the buffer amplifier reduces the effect of the buffer amplifier input capacitance and increases input dynamic range. These input attenuator advantages, however, are traded off against reduced signal-to-noise ratio.



▶ ***Figure 6.*** *First-order differential probe load model for the P7350.*

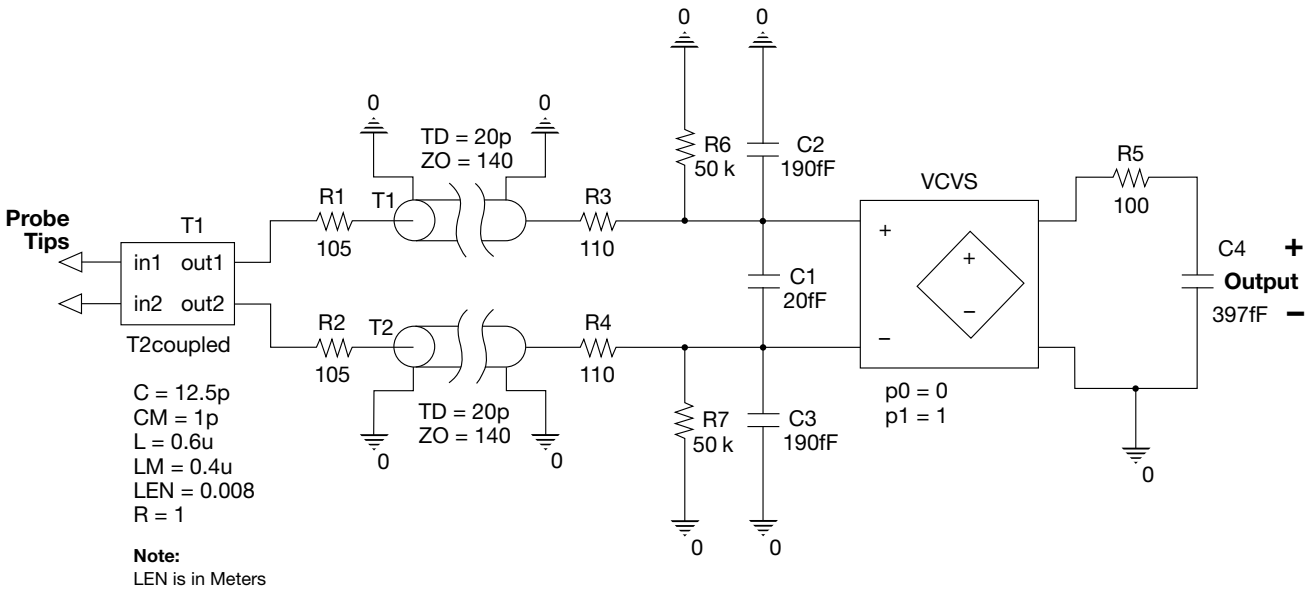
In the case of a differential probe, the probe provides a differential measurement capability at the probe tip and connects to a single oscilloscope channel input. The P7350 is a high bandwidth, differential probe with an active hybrid circuit in the probe head. The P7350 active hybrid contains a high impedance, laser-trimmed attenuator and differential buffer amplifier. By placing the buffer amplifier in the probe head, very close to the probe input pins, probe loading effects are minimized and CMRR can be maximized. The probe head is miniaturized to allow its use in physically restrictive environments and to minimize parasitics in the probe attachment path for best signal fidelity. The P7350 active probe head circuitry is powered and controlled by a TekConnect™ interface, the standard probe interface on all Tektronix high-performance oscilloscopes.

P7350 Input Loading

An ideal differential probe could be attached to a differential circuit and make measurements without disturbing the circuit under test. Any real probe, however, has a finite load impedance that may need to be accounted for in measurements, particularly at high frequencies. A first-order load model for the P7350 differential probe is shown in Figure 6. As expected, the probe load model shows a balanced structure, which to first order is identical for each of the two inputs.

The input resistor, R_I, is a damping resistor with a typical value for a P7350 probe of about 130 Ω. The common mode input capacitance, C_S, is one-half the capacitance that would be measured with the inputs shorted together, and for the P7350 probe has a typical value of about 0.4 pF. The differential mode input capacitance is the capacitance measured differentially between the two inputs, and is the sum of C_D and the series combination of the two common mode input capacitors. For the P7350 probe, which has a typical value for C_D of about 0.1 pF, this results in a differential mode input capacitance of about 0.3 pF. The common mode input resistance, R_S, for the P7350 differential probe is 50 kΩ, which results in a differential mode input resistance, R_{DM} of 100 kΩ.

This first-order probe load model provides useful information on probe loading at lower frequencies. From DC up to about 1 MHz the probe differential mode input impedance is primarily resistive, and for the P7350 probe is constant at 100 kΩ. Above about 1 MHz the probe differential mode input capacitance begins to reduce the probe input impedance until it reaches the P7350 damping resistance of 130 Ω for frequencies above 1 GHz. Although this discrete component model does provide some useful information at lower frequencies, it should be noted that the model doesn't include any probe input inductance. Neither intrinsic inductance in the probe hybrid nor attachment inductance from the probe pins or connection adapters is included in the first-order model. Probe input inductance will add resonant effects to this first order probe load



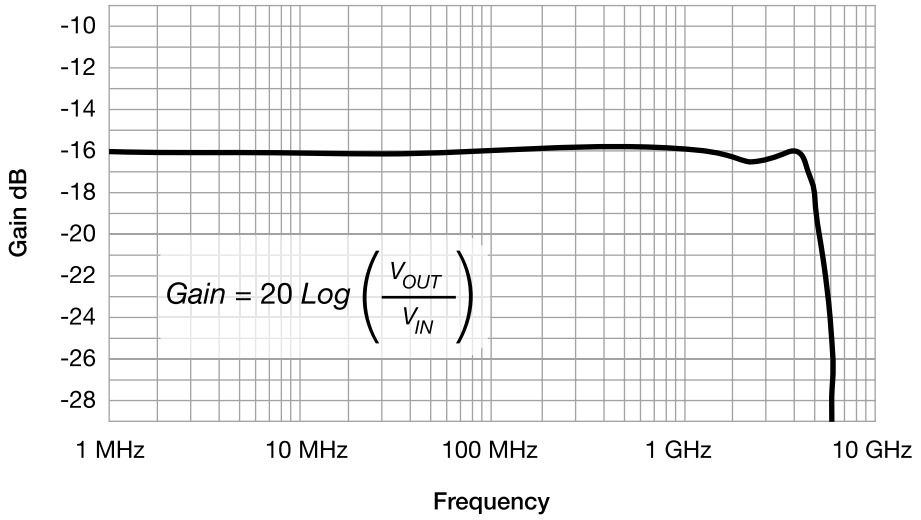
▶ ***Figure 7.*** *Distributed model for the P7330.*

model. The addition of probe interconnect adapters, which generally add more inductance to the relatively small probe pin inductance, increases probe resonant overshoot and may require additional damping resistance at the measurement node. Tektronix does provide more accurate distributed component models on its web site for most of its high performance probes, including differential probes. The distributed component model for the P7330 probe, for example, is shown in Figure 7. The P7330 probe is quite similar to the P7350 probe, but has a bandwidth specification of only 3.5 GHz. The P7330 distributed model contains a coupled transmission line input and a simplified amplifier output model with a one-pole roll-off response. This distributed component model provides accurate modeling of probe loading effects up to the limit of the probe frequency response. Although optimized for probe loading effects, the distributed component model also provides first-order transient and frequency response performance for the probe.

P7350 Amplitude Response

In order to measure an electrical signal with high fidelity, the gain of a probe amplifier must be carefully controlled over a wide frequency range. The gain of an ideal probe amplifier would be constant from DC out to frequencies near its specified bandwidth limit and then drop off fairly rapidly. The gain roll-off characteristic of this ideal probe must also be controlled to minimize pulse response aberrations. A real probe amplitude response, although designed to be flat over a broad frequency range, will exhibit some gain variation, particularly at frequencies above 1 GHz. It should be noted that the gain accuracy specification for the P7350 probe is specified as 2% at DC. The probe gain and accuracy is specified at DC primarily for convenience in measurement. Although the P7350 gain is relatively flat from DC out to about 1 GHz, as shown in Figure 8, the probe gain accuracy deviates noticeably from the DC specification at frequencies above 1 GHz. At the specified bandwidth limit of 5 GHz for the P7350 probe, for example, the gain may be rolled off as much as 3 dB, which is a reduction in gain of about 30% from the DC voltage gain.

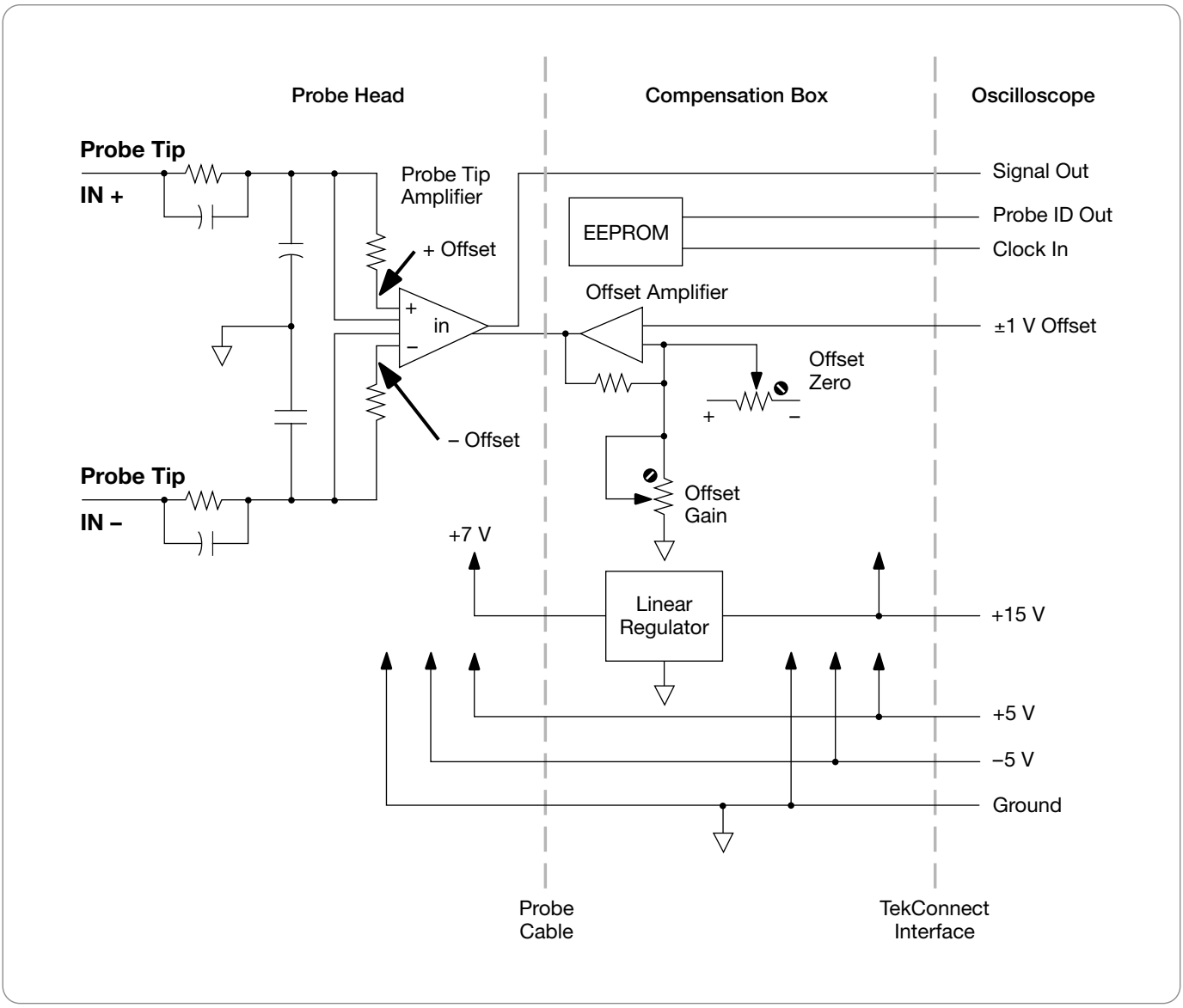
The DC voltage gain of the P7350 probe is specified to be 0.16, which represents a 6.25X attenuation of the input signal. This 6.25X probe attenuation results from the combination of the probe input attenuator and the fixed probe amplifier gain. A simplified diagram of the P7350 probe architecture is shown in Figure 9, which shows the probe input attenuator and buffer amplifier. In order to meet the



▶ ***Figure 8.*** *P7350 gain response with frequency (single-ended).*

DC gain accuracy specification of 2%, the P7350 input attenuator is laser trimmed during manufacture with its buffer amplifier active. Because of the intelligent TekConnect interface between Tektronix probes and oscilloscopes, the DC gain of the probe is usually transparent to the user. The oscilloscope automatically scales its internal gain control to match the oscilloscope vertical scale factor with the specified probe gain. Information about the probe DC gain is stored in a non-volatile memory in the probe and is read by the oscilloscope when the probe is attached. It is also possible to optimize the accuracy of the system gain and offset of the probe and oscilloscope by exercising the Probe Cal process on Tektronix oscilloscopes.

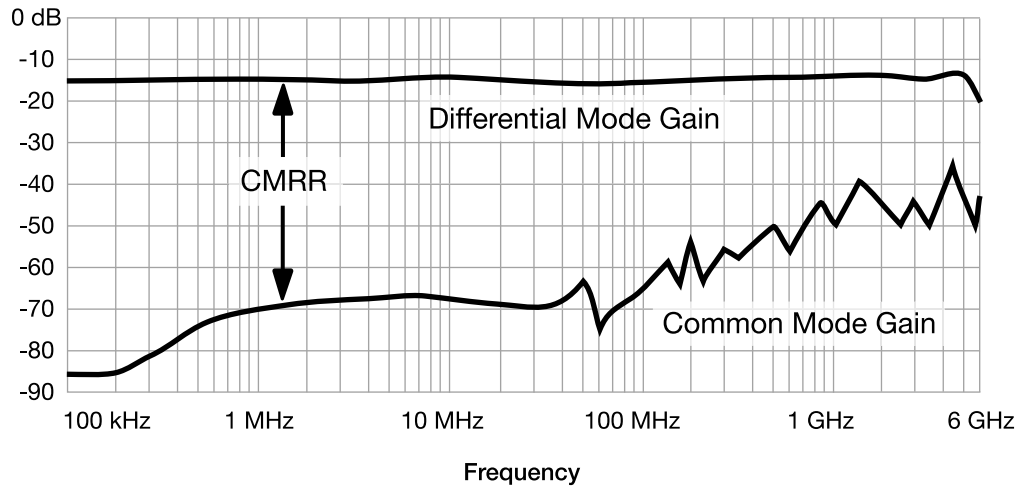
Probably the most important amplitude response specifications for the P7350 probe are its differential and common mode input range specifications. The differential mode input range represents the effective dynamic range of an input differential signal. To try to prevent inadvertent overdriving of the probe amplifier, many Tektronix oscilloscopes now show temporary annunciation markers at the dynamic range limit when the vertical scale or position is adjusted near the range limit. The differential mode input range of the P7350 probe is ±2.5 V, which is communicated over the TekConnect interface to allow the oscilloscope to set its dynamic range markers correctly. The common mode input range represents the DC voltage range with respect to ground that can be applied to both of the probe input pins without limiting the probe response. Because of the high CMRR of the P7350 probe, a common mode



▶ ***Figure 9.*** *P7350 simplified block diagram.*

DC signal within the +6.25 V and –5.0 V common mode input range will be reduced to a mV level DC offset voltage. It should be noted that the bandwidth and rise time specifications for the P7350 probe are measured with small input signals. The P7350 probe, however, has been designed to give usable speed for large signals as well. The common mode input range is not the same as the maximum non-destructive input range, which represents the input damage voltage limit of the probe. When an input signal is measured within the ±2.5 V differential signal range of the P7350 and also within its +6.25 V to –5.0 V common mode range, the signal should be processed with excellent linearity and gain accuracy by the probe buffer amplifier.

The differential mode input range of the P7350 probe can be expanded an additional ±1.25 V by applying a differential signal offset to the probe. This differential offset control is applied to the probe from the connected oscilloscope over the TekConnect interface. As shown in the simplified block diagram in Figure 9, the DC offset signal from the oscilloscope is buffered by a single-ended amplifier in the P7350 Compensation Box control board and passed to the offset input of the probe head amplifier. The probe head amplifier then converts the single-ended offset signal to a complementary differential offset signal that drives the ends of the input attenuator. The differential offset signal effectively cancels out differential DC voltages applied to the P7350 input pins. The differential offset control is perhaps most useful for single-ended



▶ ***Figure 10.*** *P7350 CMRR response.*

measurements made with the P7350 differential probe. A single-ended measurement is made with a differential probe by grounding the probe –Input pin. If a single-ended DC voltage is present at the probe +Input pin, it is effectively converted to a DC differential mode voltage:

$$V_{DIFF} = V_{+} - V_{-} = V_{DC} - 0 = V_{DC}$$

This DC differential mode voltage can be nulled out using the differential offset control, if it is within the ±1.25 V differential offset range. By nulling out this DC differential mode voltage, the P7350 dynamic range window is effectively expanded, although the ±2.5 V differential signal range limit still applies within the expanded dynamic range window.

The common mode rejection ratio (CMRR) specification for the P7350 probe is specified at several frequencies from DC to 1 GHz. CMRR is defined as the ratio of differential mode gain to common mode gain. CMRR is effectively a measure of how well matched the two differential signal paths of the probe input have been designed and manufactured. Path mismatch, particularly at higher frequencies, can cause some of the differential mode signal to be converted to a common mode signal, which reduces CMRR. Because of increasing parasitic effects with increasing frequency, CMRR drops off with frequency as shown in Figure 10. On the log-scale display of differential mode and common mode gain over frequency in Figure 10, CMRR can be calculated by simply subtracting DM gain in dB from CM gain in dB at any frequency:

$$CMRR = A_{DM}(dB) - A_{CM}(dB)$$

The CMRR performance of the P7350 probe is measured with a network analyzer, which has a very controlled impedance environment. The CMRR that is observed in an actual differential measurement application will be affected by signal source and load impedance mismatch as well as differential signal skew and other routing variations.

P7350 Timing Response

The two key timing response parameters for an oscilloscope probe are bandwidth and rise time. Bandwidth is a frequency domain representation of a probe's timing performance and is defined as the frequency at which the probe DC gain has fallen by 3 dB. Rise time is a time domain representation of a probe's timing performance and, in general, is defined as the time interval between the 10% and 90% crossing points on a step (pulse) waveform. Although for a known signal response characteristic there is a fixed relationship between bandwidth and rise time, the response of high-speed probe amplifiers varies enough that the traditional bandwidth-rise time product of 0.35 for a Gaussian amplifier is not very accurate. Because an oscilloscope is fundamentally a time domain instrument, Tektronix guarantees probe rise time performance and specifies probe

bandwidth as typical. Although probe bandwidth may be a typical specification, it is nevertheless a measured rather than a calculated parameter for Tektronix probes and has well defined manufacturing quality limits.

The bandwidth of the P7350 differential probe is specified as DC to ≥5 GHz. Bandwidth is specified as a typical, probe-only specification. It is measured using a doubly terminated probe test fixture, which results in an effective 25 Ω source impedance. For ease in manufacturing, bandwidth is currently made as a single-ended measurement using a network analyzer with one probe pin grounded. Differential mode bandwidth performance has been verified however using mixed mode S-parameter methods. Although the measurement system bandwidth when using a P7350 depends on the bandwidth of the host oscilloscope, the traditional root-mean-square calculation combining the oscilloscope bandwidth and the probe-only bandwidth should not be assumed valid. The intelligent TekConnect interface allows TekConnect oscilloscopes to identify the attached probe type and take control measures to optimize the system bandwidth. The P7350 probe when used with the 6 GHz TDS6604 oscilloscope, for example, has a system bandwidth of 5 GHz, limited largely by the probe response. Similarly, the P7350 probe when used with the 4 GHz TDS7404 oscilloscope has a system bandwidth of 4 GHz, limited in this case by the oscilloscope bandwidth. In both of these cases, the system bandwidth is better than expected, based on a root-mean-square calculation combining the probe-only bandwidth and oscilloscope bandwidth.

The 10–90% rise time of the P7350 differential probe is specified as ≤100 ps. Rise time is specified as a guaranteed, probe-only specification. It is measured using the same doubly terminated probe test fixture used for bandwidth measurement. Because the system rise time of the applied pulse source and sampling oscilloscope used to measure probe rise time is only about 30 ps, the probe rise time must be extracted from the measurement using a root-mean-square calculation:

$$\text{rise time}_{probe} = \sqrt{(\text{rise time}_{system\&probe}^2 - \text{rise time}_{system}^2)}$$

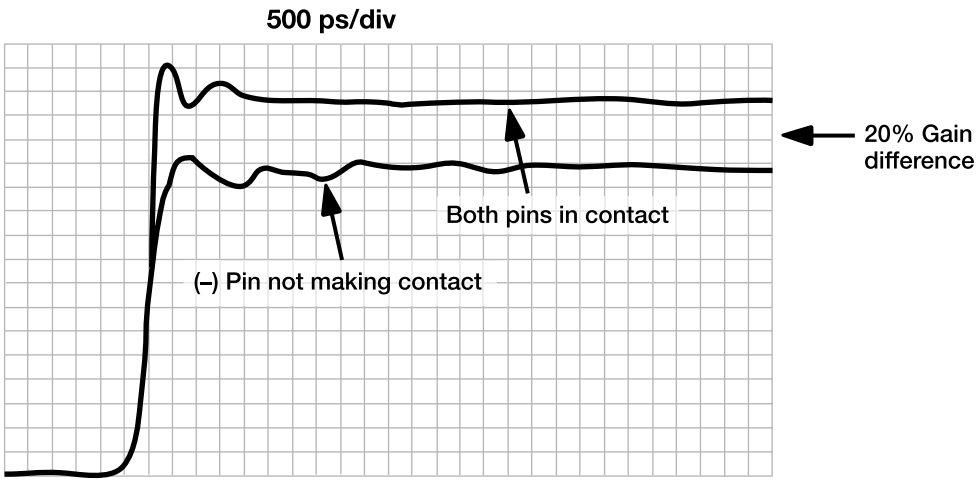
Since many serial data standards now specify 20–80% rise time measurements, the P7350 has specified a typical 20–80% probe rise time of ≤65 ps. This value, which has been verified thoroughly with probe testing, also agrees with the general rule of thumb relationship between 10–90% rise times and 20–80% rise times:

$$RT_{10-90} \approx 1.5 * RT_{20-80}$$

Differential Probe Attachment Issues

One of the critical probing issues in making accurate measurements of high-speed signals is the probe attachment to the circuit-under-test. Any high bandwidth active probe, whether differential or single-ended, will only provide full bandwidth performance when the measurement nodes are connected to the probe input pins with short leads. The use of long connection leads on a probe input adds parasitic inductance and capacitance that either reduces the probe bandwidth or produces resonant effects. Attaching a probe to a circuit using long connection leads will thus cause the signal being measured to appear distorted. Part of the distortion seen may actually be real, caused by disturbance of the measured circuit by the loading of probe and connection parasitics. Even if the probed circuit is not affected noticeably by the parasitic measurement load, the interconnect parasitics may still distort the measurement of the probed signal. These parasitic problems from long connection leads become worse as the rise time of the measured signals becomes faster. Even the use of higher bandwidth probes, which generally have lower input parasitics at the probe tips, will not help much if significant parasitics are added to the measurement by using long connection leads. The attachment of probe connection adapters also may increase measurement parasitics, although the use of adapters may be the only way that contact can be made to some circuits.

Another important probe attachment issue is the reliability and repeatability of the measurement. In the case of single-ended measurements, the quality of the ground lead connection is often the primary factor in connection repeatability. Since single-ended probes are generally designed with an asymmetrical structure, the connection focus is often on making a solid contact between the probe input pin and the circuit signal. The probe ground requirement for low-speed signals is to simply locate a convenient ground point somewhere on the circuit board. For high-speed signals, however, the ground connection can be as critical as the signal connection for good measurement fidelity. A high-speed ground connection should be as short as possible and should be attached to a low inductance ground reference close to the signal connection. A short ground connection is important not only to minimize interconnect parasitics, but also to reduce inductive noise pickup by the probe grounding loop. The sensitivity of single-ended measurements to ground noise can sometimes result in measured signal variation when different ground nodes are contacted near the measured signal node. Single-ended measurements are also sometimes affected by the physical location of the handhold on the probe, since body capacitance contributes to the overall probe interconnect parasitics. The issue of probe lead mechanical attachment compliance is usually handled by spring action in



▶ ***Figure 11.*** *Differential probe contact error.*

the ground lead. This can be done using a pogo-pin ground lead when the correct probe spacing between signal and ground points on the probe has been designed into test points on the circuit board. For the more general case, a flexible z-ground lead can be used or a customizable ground lead can be soldered to a ground reference near the signal point and then plugged into the probe ground socket.

Differential Probe Attachment

In the case of differential probe attachment, there are two signal inputs and also a ground lead connection point on the side of the probe head. Because of the high CMRR of a differential probe, the requirements for a ground connection are very different than for a single-ended probe. In general, it is not necessary to make a ground lead connection to a differential probe when making measurements. In fact the addition of a ground lead connection from a differential probe to the circuit ground may actually inject noise into the measurement. When a differential probe is used to make a single-ended measurement, the circuit ground connection should be made with the differential probe negative input pin rather than the probe head ground lead connection. The only application where a differential probe head ground connection is necessary is with earth ground isolated circuits such as battery-powered devices.

One of the more challenging attachment issues in the use of differential probes is probe lead connection compliance. Because differential probes have two identical input pins, making reliable connection to circuit contacts with both pins at the same time is generally more challenging than with single-ended probes. As noted earlier, a single-ended probe structure is usually asymmetrical, making the addition of connection compliance to the ground pin an easier task than with a differential probe, where symmetry must be preserved for good CMRR. Although some lower performance differential probes have sockets on their inputs, the present generation of high performance differential probes, such as the Tektronix P6330, P7330, and P7350, use solid male pins as input leads. Input pin sockets generally provide more flexibility in measurement applications by allowing the easy attachment of different adapters. Male input pins are used on higher performance probes, however, because of reduced parasitics compared to pin sockets. The problem of attaching adapters to male input pins has, however, been solved by the use of elastomeric contacts in the probe tip adapters.

Because of the connection compliance problem with differential probes, care should be taken so that subtle measurement errors are not made. An example of the kind of error that can occur because of poor differential probe pin contact is shown in Figure 11. The two waveforms in Figure 11 show that it is possible to make a measurement that appears to have the correct waveform shape when only one of the two differential input pins makes solid contact with the circuit.

The single pin contact measurement, however, shows a large gain error, a slower rise time, and long-term signal distortion, when compared to a correct two pin contact measurement. One method that can help with differential probe attachment compliance is the use of probe positioners, such as the Tektronix PPM100. Since they have been designed for hands-free probing, probe positioners have also been designed to solve the probe attachment compliance problem. The PPM100 probe positioner addresses the attachment compliance problem with coarse and fine position adjustment controls and flexible probe retention rings. The flexible probe retention rings that attach the probe to the probe holder arm also provide some spring action in holding the probe in solid contact with the circuit.

The use of solid male pins on differential probe inputs also encourages planning for measurement test points with the correct probe pin spacing on circuit boards. Ideally, critical measurement nodes should be identified and pads added for probing to give the best measurement performance. Realistically, however, not all measurement nodes can be identified in advance, and it becomes more and more difficult to add probing pads to high-speed circuits without introducing significant parasitic loading to the circuit, even without the probe attached. Trying to probe a pair of differential traces having less than 10 mil width and spacing with differential probe pins having a fixed 100 mil spacing is of course not possible. A variety of probe tip adapters have been developed by Tektronix to try to address this probe attachment challenge.

Although there is a long list of probe tip adapters available for use with Tektronix differential probes, the primary adapters used for high-speed differential probing are the

- Variable spacing adapter
- Square pin adapter
- Solder-in adapter

All three of these adapters are designed to slip over the probe tip housing of a differential probe with male pins like the P6330, P7330, or P7350. Electrical connection between the probe pins and the adapter pins is made with elastomeric contacts inside the adapter housing. The elastomeric contacts used in Tektronix male pin adapters are rated for 50-75 insertion cycles. For reliable operation an adapter must be pushed fully onto the probe tip housing until it seats against the probe head. These adapters are also polarized, requiring an alignment between the +Input and –Input pins on the differential probe tip housing and the matching + and – markings on the adapter housing.

Variable Spacing Adapter

The variable spacing adapter is designed to expand the range of probe pin access between any two circuit points from 20 mils to 180 mils apart. The pins on the variable spacing adapter rotate in their housing to provide this range of contact. The articulated pins should be handled gently and it is recommended that they be rotated using a pair of tweezers. Although the variable spacing adapter pins can be bent, they are somewhat fragile and adapter pin bending should be done only with great care. The male pins on the differential probe itself are designed for strength not flexibility and should never be bent. Although the use of the variable spacing adapter will not generally degrade the probe rise time, the added inductance will increase the aberrations measured with a very fast rise time pulse when compared with no adapter. This is a difficult effect to quantify, because the degree of aberrations observed is dependent on not only the probe response characteristics, but also on both the input signal rise time and aberrations. Input signals having a rise time slower than the specified probe rise time will exhibit smaller aberrations than a fast rise time signal. Slower rise time signals effectively have less high frequency energy to excite the probe interconnect resonance.

Square Pin Adapter

The square pin adapter is designed to allow probe attachment to 25 mil square pins spaced 100 mils apart. The square pin adapter also allows other probe tip accessories to be attached to extend the reach of probe contact beyond that possible with a variable spacing adapter. Although the response of the square pin adapter with short square pins attached is similar to that of the variable spacing adapter, the addition of longer lead length without additional damping resistance will make the measurement response more resonant, increasing the aberrations seen with fast rise time pulses. Adding damping resistance to longer lead connections from the square pin adapter will reduce the size of measurement aberrations, but will also reduce the measurement bandwidth significantly.

Although recent introductions of some competitive probe offerings have made the use of a damping resistor at the probe attachment point sound like a revolutionary development, Tektronix has always included a damping resistor at the input pins of its active probes. This damping resistor has been chosen to provide optimum pulse response with very short probe attachment connections, which is the configuration with the highest frequency response. It is true, however, that longer, non-optimum probe attachment connections

Table 4. P7350 Soldered-in Adapter Response Characteristics (100 ps input step)

Connection Type and Length	Bandwidth	Rise Time 10/90%	Rise Time 20/80%	Overshoot
Probe only (ref)	>5 GHz	127 ps	85 ps	10%
Wire, 0.050"	>5 GHz	114 ps	77 ps	14%
Wire, 0.100"	>5 GHz	111 ps	76 ps	22%
10 Ω, 0.050"	4.5 GHz	120 ps	81 ps	18%
10 Ω, 0.100"	4.0 GHz	120 ps	81 ps	21%
20 Ω, 0.050"	4.2 GHz	129 ps	87 ps	9%
20 Ω, 0.100"	3.9 GHz	128 ps	87 ps	13%

will result in overshoot and possibly ringing in the probe response. This measurement distortion is due to the input capacitance of the probe resonating with the probe attachment inductance. By adjusting the damping resistance value and to some degree its location in the probe attachment topology, it is possible to preserve a relatively flat pulse response by trading off bandwidth for probe attachment lead length.

Solder-in Adapter

The solder-in adapter is designed to allow the creation of a customized, hands-free connection to a differential signal and to facilitate the addition of external damping resistance. The use of a soldered contact to the circuit also provides a more reliable and repeatable connection than is generally possible with differential probe pin connections made with hand pressure. The solder-in adapter looks very similar to the square pin adapter, but contains sockets for small diameter wires and can be damaged if 25 mil square pins are inserted. A resistor/wire kit is supplied with the solder-in adapter that contains small diameter wire leads and leaded resistors fitted with small diameter leads. For additional flexibility, the kit also contains wires and resistors to allow connection to small circuit board vias. The solder-in adapter kit should be checked for the specific wire diameter range supported by the adapter sockets. The adapter side of the resistor leads has been pre-cut so that the resistor body touches the adapter socket when fully inserted in order to minimize parasitics. The circuit side of the resistor leads should be cut as short as possible when making a circuit connection and should be cut symmetrically to preserve probe CMRR. Because of the small physical size of the soldered connections, it is recommended that adhesives be used to secure the resistors or wires to the circuit board. Where possible the probe should also be temporarily taped to the board when measurements are made to relieve strain on the adapter and soldered connections. A probe positioner, such as the PPM100, can also be used to provide mechanical support for the probe and solder-in adapter. The resistors supplied with the solder-in adapter kit are 1% metal film resistors. Because Tektronix differential probes already contain a damping resistor in the probe tip hybrid, only small value, 10 Ω and 20 Ω resistors are supplied with the kit. The choice of using a wire or resistor for the soldered connection to the circuit depends on the length of the connection. Table 4 shows typical electrical characteristics of a soldered-in adapter when used with a P7350 probe. The table shows that for the soldered-in adapter, as the length of a wire connection increases, the connection becomes more resonant and the pulse response overshoot increases. The table also shows that connection resonance for longer lead lengths can be damped out by using either the 10 Ω resistor or the 20 Ω resistor rather than a wire to make the soldered connection. The trade-off that must be made for longer lead length and more damping is reduced bandwidth, as is also shown in the table.

Alternate Measurement Methods

Although it might seem obvious that single-ended measurements should be made with single-ended probes and differential measurements should be made with differential probes, alternative measurement methods are commonly used. It is certainly possible, for example, to make single-ended measurements with a differential probe. It is similarly possible to make differential measurements using a pair of single-ended probes and oscilloscope waveform math. It is also possible, in a 50 Ω signaling environment, to make single-ended or differential measurements without probes. The signals in a 50 Ω signaling environment are terminated by the 50 Ω inputs on the measurement equipment. Signals in a 50 Ω signaling environment are directly cabled to the 50 Ω inputs available on all high-performance oscilloscopes, both real-time and sampling. The differential signal response is then computed by subtracting the two channel inputs using the waveform processing feature of the oscilloscope. A unique approach to making differential measurements in a 50 Ω signaling environment has been introduced by Tektronix with the P7350SMA probe. The P7350SMA probe can be used to make a differential measurement in a 50 Ω signaling environment on a single oscilloscope channel. The P7350SMA probe contains a differential input termination network as well as a high performance differential buffer amplifier. Each of these alternative measurement methods will now be examined in some detail in this final section of the primer.

Single-ended Measurements with a Differential Probe

One of the common misconceptions about the use of differential probes is that they can only be used for measuring differential signals. In fact, the high CMRR of a differential probe means that a differential probe can generally be used to make single-ended measurements with high-signal fidelity. The low-input capacitance of high-performance differential probes like the Tektronix P6330, P7330, and P7350 results in reduced circuit loading and may actually provide superior signal fidelity compared to single-ended probes of similar bandwidth. In addition, since differential probes make their single-ended measurement ground connection with one of their high impedance input pins rather than a low impedance ground lead, they seem to be less susceptible to noise injected into the measurement ground loop. This common mode noise rejection characteristic of a differential probe also results in less sensitivity to the physical placement and handling of the probe.

Single-ended measurements of differential signals are very important in differential signal testing since they can identify possible asymmetry between the two differential signal pairs that cannot be separated out in a differential measurement alone. When a differential probe is used to measure an ideal complementary differential signal, the common mode component of the signal is a DC voltage, which is largely rejected by the high DC CMRR of the probe. When the differential probe is then used to make a single-ended measurement of one of the complementary signals, the common mode component of the signal has both an AC and DC response. When measured with a differential probe, the common mode component of a single-ended signal is equal to one-half the signal amplitude.

$$V_{CM} = (V_+ + V_-)/2$$

$$V_+ = \text{single-ended signal}$$

$$V_- = \text{OV (ground)}$$

If the CMRR of the differential probe is not large enough, then some of the common mode signal will bleed through and distort the output signal. This common mode bleed-through problem is worse at high frequencies where parasitic mismatches tend to reduce CMRR. The differential mode component of the single-ended measurement is also only half that of a differential measurement on a complementary signal. As a result of this smaller signal, the error from common mode bleed-through appears relatively larger as well. Even though there may be a common mode error term present in a single-ended measurement made with a differential probe, it will be small for a probe with good CMRR. In addition, the error term may be smaller than the ground noise error signal present in a single-ended measurement using a single-ended probe.

Pseudo-differential Measurements

Differential measurements made using two single-ended probes and oscilloscope waveform math are commonly referred to as pseudo-differential measurements. Pseudo-differential measurements can be made with either real-time or sampling oscilloscopes. Depending on the measurement signaling environment, pseudo-differential measurements can be made with either cables or probes. Cables can be used in the case of serial data compliance testing, where the transmitted signal is in a 50 Ω signaling environment and the signal path can be broken and terminated at the ground-referenced, 50 Ω oscilloscope input. High impedance probes must be used where the signal path cannot be broken or where debug of the signal must be done at any of a number of places along the signal path. Because of the difficulty of matching the signal paths in two separate oscilloscope channels, the CMRR for pseudo-differential measurements tends to be somewhat poorer than that of a good differential probe. Differential probes are carefully designed for differential signal path matching in order to optimize CMRR. As a result, pseudo-differential measurements may exhibit less signal fidelity than measurements made with a good differential probe, although other factors such as amplitude response and circuit loading can also affect the fidelity of the measurement. Pseudo-differential probing, of course, requires more oscilloscope channels per differential signal than needed by a differential probe.

Sampling oscilloscopes are often chosen for pseudo-differential measurements made in a 50 Ω signaling environment because of the high bandwidth of a sampling system. The measurement fidelity of a sampling system also tends to be superior, with less signal reflection problems and excellent noise performance. A sampling oscilloscope, however, requires a periodic signal, which makes it more difficult to use for debugging transient problems. It is also impossible to use a sampling oscilloscope for capturing and analyzing a real-time data stream, as is required for jitter testing of data signals in some of the serial data standards such as PCI Express. A sampling oscilloscope also generally requires an external trigger signal, such as a data rate clock, which is not always readily available. High-performance real-time oscilloscopes are now available with high enough bandwidth and sampling rate to be effectively used in high-speed serial data measurement applications. Real-time oscilloscopes also provide triggering on the input data signal, including the capability on some Tektronix oscilloscopes to trigger on a specific serial data pattern, including internal clock recovery triggering.

Since pseudo-differential measurements are made using two different measurement signal paths, the measurement path amplitude response and timing delays must be closely matched for high measurement fidelity. Amplitude response mismatch and signal delay variation between the two oscilloscope channels will usually set the fundamental CMRR limit for a pseudo-differential measurement. Care should be taken, however, so that interconnect mismatch between the signals to be measured and the oscilloscope channels is minimized. If the two signal input paths are not carefully matched, then interconnect path differences will distort the response. Identical cables or probes, with matched response and time delays, should be used for pseudo-differential measurement interconnections. When cables are used for signal interconnect, delay variations are primarily determined by variations in cable length, with a typical signal delay of about 150 ps/inch for commonly used 50 Ω coaxial cables. Probe delay variations are affected by differences in both probe cable length and probe head amplifier delay, with the probe-to-probe delay for the P7350, as an example, specified to be a maximum of 600 ps. Real-time oscilloscope channels also exhibit signal path delay variations from the input to the acquisition sampler. There can be a timing variation of several hundred picoseconds between channels of an oscilloscope, as well as a similar delay variation between attenuator paths of a single channel. Sampling oscilloscopes have delay variation between channels, particularly channels on different sampling modules, but have no attenuator path delay variations because they have no input attenuators.

Measurement Channel Deskew

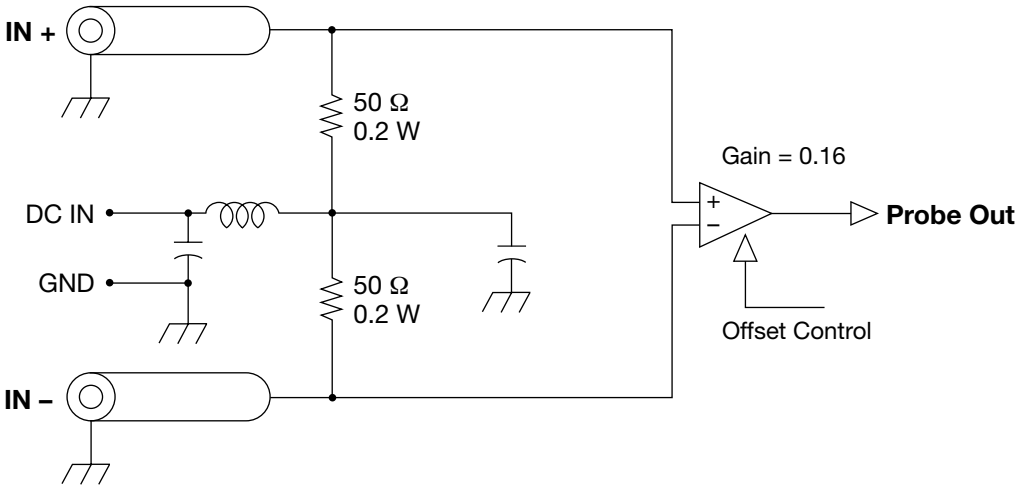
Both sampling and real-time oscilloscopes require a channel deskew procedure to compensate for delay differences between the two measurement channels and the attached cables in a pseudo-differential measurement. Deskewing two TDS8000 sampling oscilloscope channels requires two sampling modules. Even though many of the TDS8000 electrical sampling modules are dual channel, the sampling architecture only provides one trigger strobe per module. Although this architecture provides excellent timing alignment between the intra-module channels, only inter-module channels can be deskewed with time-aligned channels. Although the TDS8000 sampling oscilloscope controls will allow an apparent deskew of intra-module channels, the timing adjustment between channels actually takes place on alternate acquisitions. Acquiring the two pseudo-differential signals on alternate acquisitions results in time alignment problems with the computed differential signal for common eye pattern signals. Deskewing channels on a TDS8000 sampling oscilloscope is done from the vertical setup menu, using the Channel-deskew control. The deskew channel procedure can be found in the Optimizing Measurement Accuracy section of the TDS8000 User Manual.

Unlike sampling oscilloscopes, deskewing channels on a high-performance real-time oscilloscope can be done on any set of channels without concern for time aligned waveform problems. Many high-performance real-time oscilloscopes, however, have maximum real-time sampling rate limitations that may affect the choice of channels used in making pseudo-differential measurements. The 6 GHz TDS6604 oscilloscope, for example, can sample at 20 GS/s for dual channel acquisitions, but only for certain channel combinations, such as CH1 and CH3. For some dual channel and all quad channel acquisitions, the maximum real-time sampling rate drops to 10 GS/s. Since the greatest signal fidelity is obtained with the maximum sampling rate, pseudo-differential measurements should use channel combinations that sample at the highest rate.

The TDS6604 oscilloscope specifies a maximum skew of 30 ps between two channels with the same vertical scale factor and coupling. Additional skew is introduced with either cables or probes used to interconnect to the differential signal paths. Deskew of channel timing in the TDS6604 oscilloscope is done with controls in the vertical setup window. The deskew channel procedure can be found in the Optimizing Measurement Accuracy section of the TDS6000 Series User Manual. The deskew procedure requires a high-speed signal edge that is connected in common to both differential signal interconnects. In the case of two probes, Tektronix provides a Probe Deskew Fixture that generates a fast edge signal and convenient probing points. For the case of cables, obtaining a pair of tightly matched delay signals is generally more difficult, since a fast edge signal in a 50 Ω environment is susceptible to serious distortion problems unless care is taken in splitting the signal between the two paths. Although a 50 Ω power splitter is often used in this application, the use of a dual TDR sampling module like the Tektronix 80E04 provides a more controlled set of matched delay, fast edge signals. No matter what signal source is used for the deskew signals, the TDS6604 oscilloscope should be configured to the vertical and horizontal scale settings that will be used in the measurement application. Changing the vertical scale factor or horizontal scale factor after deskewing the channels can result in a significant variation in timing accuracy between the channels, which will almost certainly increase the channel skew.

Differential SMA-input Probe

Tektronix' P7350SMA probe has a unique architecture optimized for serial data compliance testing and other high-speed differential measurement applications. The P7350SMA probe fulfills the increasing need for differential to single-ended signal conversion in a 50 Ω signaling environment using a single oscilloscope channel input. The use of SMA connectors provides a reliable, repeatable signal attachment method for compliance testing, where the signal path can be interrupted and terminated at the measurement input. In addition, through the use of an embedded differential amplifier, the P7350SMA probe provides its differential measurement interface at the end of a 1.2 m cable rather than at the oscilloscope front panel. This brings the differential measurement interface closer to the circuit-under-test, which minimizes frequency dependent cable interconnect losses.



▶ ***Figure 12.*** *P7350SMA probe architecture.*

The P7350SMA probe architecture, as shown in Figure 12, includes dual SMA connector inputs, a dual 50 Ω resistor termination network, a common mode DC bias connection to the termination network, and an embedded differential amplifier. The SMA inputs provide a reliable connection interface for high-frequency, 50 Ω signal paths to the embedded differential amplifier and input termination network. The probe input termination network is implemented in a shielded module that utilizes laser-trimmed hybrid circuit technology to provide high bandwidth, good power dissipation, and excellent CMRR performance. The input termination resistors are coupled together with a common mode termination network that is designed to provide a low impedance path to ground. The DC bias connection to the common mode termination network is made from a user-supplied, external DC power supply through a dual banana plug connector on the probe. The embedded differential amplifier provides 5 GHz bandwidth, 6.25X attenuation, and a set of amplitude and timing specifications similar to a conventional P7350 probe.

The input termination network is designed to provide broadband 50 Ω terminations for both common mode signal pairs of a differential signal. For an ideal, complementary differential signal, there is only a DC common mode component and the termination resistors alone should terminate the signal with minimal reflections. A practical differential signal, however, has both amplitude and timing mismatch, which results in an AC common mode component. The input termination network includes a common mode capacitance at the node between the termination resistors, which provides a common mode termination for high-frequency signals. The common mode capacitance of approximately 0.02 uF for the P7350SMA termination network holds the common mode node impedance below 1 Ω down to a breakpoint frequency of about 7 MHz. The common mode node impedance breakpoint frequency can also be shifted all the way down to DC by driving the DC bias input from a low resistance DC source.

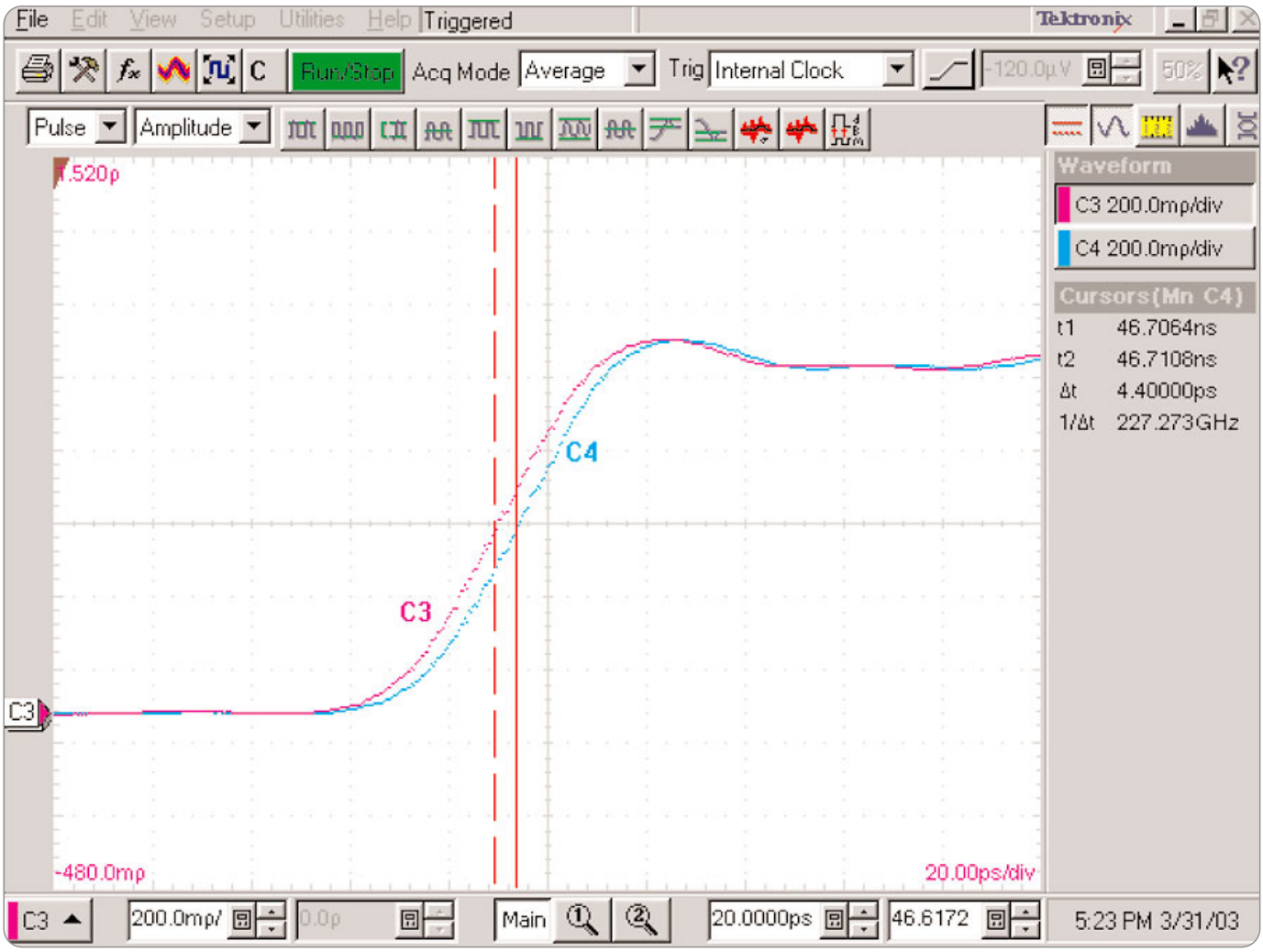
When used to measure a high-speed, complementary differential signal that has no need for a common mode DC termination voltage, the P7350SMA probe can be used with the DC bias port open. This is generally the safest configuration for the P7350SMA probe, since there is less risk of exceeding the 500 mW power limit of the 50 Ω termination resistors. Some common high-speed logic circuits, however, are designed to operate properly only with their termination resistors connected to a specified DC termination voltage. The LVPECL logic family, for example, when operated from a 3.3 V power supply is designed to operate with its output termination resistor connected to a 1.3 V pull-down voltage. The conventional method for characterization testing of an LVPECL device requires the test board to be powered from split power supplies, (e.g., +2.0 V and –1.3 V), so the outputs could be terminated with 50 Ω to ground at an oscilloscope channel input. The DC bias input of the P7350SMA probe should allow testing of LVPECL circuits without the use of split power supplies. A P7350SMA probe can similarly be used for testing a CML logic output, where the DC bias input provides the CML termination resistor pull-up voltage. Care should be taken when using the DC bias input of the P7350SMA probe so as not to exceed the 500 mW power rating of the probe termination resistors. Since the termination power is a function of both the probe input signal voltage and the probe DC bias voltage, a maximum DC bias voltage specification is not sufficient. In the special case where the probe input signal is a DC voltage, the voltage difference between either probe SMA input and the DC bias input should be kept less than 5.0 V so as not to exceed the 500 mW power rating of the termination resistors. Equations have been provided in the P7350SMA User Manual for calculating power dissipation in the termination resistors for a complementary differential signal.

Although designed and specified primarily for use in making differential signal measurements, the P7350SMA probe can be configured to make single-ended measurements. Single-ended measurements can be made using the P7350SMA probe by connecting the single-ended signal to the +Input of the probe and terminating the –Input of the probe with a 50 Ω SMA termination resistor. A pair of SMA termination resistors is supplied with the P7350SMA probe to protect the probe inputs and for possible use in making single-ended measurements. When used to measure a high-speed serial data signal with limited low frequency power below 10 MHz, the common mode capacitance effectively terminates the single-ended signal input and, as a result, the DC bias port can be left open. Most gigabit serial data signals with 8B/10B encoding meet this low-frequency spectral requirement and thus can be used without a DC bias connection. The exception to this general rule is where the signal driver requires a common mode DC termination voltage. A dual banana plug, shorting strap is also supplied for use on the DC bias input when doing a Probe Cal on the P7350SMA. Since the Probe Cal signal on TekConnect oscilloscopes is a DC voltage during a Probe Cal operation, the short to ground is needed to force the probe –Input to ground for proper operation.

Although the timing skew between the inputs of the P7350SMA probe at the SMA connectors is typically <1 ps, additional skew in the differential signal path due to interconnect cables must be carefully controlled. A pair of low-loss, matched delay SMA cables is supplied with the P7350SMA probe for general-purpose interconnect use. These 12 inch long cables are strapped together as a cable assembly because of their matching delay and are tested for a guaranteed skew <10 ps. Low-loss, but flexible, coaxial cable is used in this cable assembly, with a specified insertion loss <1.0 dB to 18 GHz, which results in a typical insertion loss to 5 GHz of <0.5 dB. One indication of the effect of input skew on high-speed differential signal measurements is shown in the rise time data in Table 5. The TDR deskew control on a Tektronix 80E04 TDR sampling module was used to intentionally add skew between the fast rise time pulse edges of a differential TDR signal. The differential TDR signal was then measured with a P7350SMA probe and the effect of varying the skew over about a ±100 ps range was observed. The fastest rise time was measured when the skew was minimum. The rise time of the signal output from the P7350SMA probe remained within a few picoseconds of its fastest value for skew <±10 ps. As the skew was made larger than ±10 ps, the rise time of the probe output continued to slow until the skew reached about ±50 ps. With the skew more than ±50 ps, distortion in the output edge became noticeable, eventually resulting in a double-stepped edge. The skew at which the distortion in the pulse step first becomes visible seems to be a combination of the rise time of the TDR signal (about 30 ps) and the specified rise time of the probe (<100 ps). This seems reasonable, since the measured rise time of the probe is also a combination of the rise time of the signal and the specified rise time of the probe. Although the data in Table 5 seems to imply that there is little effect on a measured differential signal for skew <±10 ps, it should be remembered that the data in this table applies only to measured pulse rise time. It should be expected that a skew of ±10 ps might have a more noticeable effect on other differential signal measurements, such as the crossover point of a high data rate eye pattern.

Table 5. P7350SMA Rise Time Variation with Input Skew

Input Signal Skew (differential TDR)	Rise Time (10-90%)
–100 ps	253 ps (distorted)
–75 ps	206 ps (distorted)
–50 ps	141 ps
–25 ps	106 ps
–10 ps	97 ps
0 ps	94 ps
5 ps	95 ps
10 ps	96 ps
15 ps	98 ps
20 ps	101 ps
25 ps	104 ps
30 ps	110 ps
35 ps	116 ps
40 ps	125 ps
45 ps	133 ps
50 ps	142 ps
75 ps	213 ps (distorted)
100 ps	264 ps (distorted)



▶ ***Figure 13.*** *P7350SMA matched cable delay.*

If the skew of the matched delay cable set supplied with the P7350SMA probe is not small enough to meet the requirements of an application, it is possible to manually deskew the cables using a pair of mechanical SMA Phase Adjusters. SMA Phase Adjusters are available from Tektronix as an optional accessory to the P7350SMA probe. Before adding a pair of SMA Phase Adjusters to the matched delay cable assembly, it is prudent to measure the actual skew of the cables, since it may be smaller than the guaranteed spec of <10 ps. Measured results showing a low enough cable skew may remove the need for manual deskew of the cables, except perhaps when very low skew characterization must be done. Cable skew can be measured using TDR measurement equipment. Figure 13 shows a TDR delay measurement made on a cable set connected to a Tektronix 80E04 TDR Sampling Module in a TDS8000 sampling oscilloscope. It should be noted that the cable skew measured using TDR methods needs to take into account the fact that displayed TDR delays represent down and back delays. As a result, measured skew will be one half the down and back TDR reflected delay. The skew measured using cursors shown in Figure 13, for example, is 2.2 ps. Although the SMA Phase Adjuster has a limited adjustment range of only 25 ps, that should be sufficient to deskew the matched cable set supplied with the P7350SMA probe. It should be noted that manually deskewing the matched delay cable set requires two SMA Phase Adjusters in order to match the Phase Adjuster insertion delay of about 450 ps in each signal path. The use of an SMA Phase Adjuster in each cable also tends to match the Phase Adjuster loss characteristics in each signal path. A procedure for manually deskewing the matched delay cable set using SMA Phase Adjusters can be found in the P7350SMA User Manual.

Each of the alternate measurement methods described for making differential measurements has advantages and disadvantages. Pseudo-differential measurements with a sampling oscilloscope might be the method of choice because of the need for the highest bandwidth available. Pseudo-differential measurements with a high-performance real-time oscilloscope might be the method of choice because of the need for a long record length real-time acquisition and the availability of a pair of high bandwidth single-ended probes. The use of a pair of P7350SMA probes might be the method of choice because of the need to make lane-to-lane skew measurements between several differential serial data lanes. One factor that should be considered in evaluating the use of these alternate measurement methods is their CMRR performance. As was described earlier, CMRR response, not just at DC, but over the full frequency range of operation, is one of the critical parameters for making differential measurements with high signal fidelity. The CMRR performance of the P7350SMA probe is specified and guaranteed at a number of frequency points. The CMRR performance for pseudo-differential measurements is generally not specified for either real-time or sampling oscilloscopes. The large variety of possible channel combinations and the need for deskew over a wide range of vertical and horizontal settings makes specifying CMRR for oscilloscopes very difficult.

The CMRR performance for a specific pseudo-differential measurement setup can, however, certainly be measured. It is relatively easy to make DC CMRR measurements of a pseudo-differential setup, because a DC signal can be split without reflection problems. AC CMRR measurements are more difficult to make, however, particularly for bandwidths greater than 1 GHz. One possible method for making AC CMRR measurements of a pseudo-differential measurement setup uses a dual TDR pulse source like the Tektronix 80E04 TDR Sampling Module. Since the 80E04 can generate both differential mode and common mode pulse signals, it can be used to produce both differential and common mode responses in the pseudo-differential measurement setup. By differentiating the differential mode and common mode pulse response waveforms and performing an FFT on the resulting impulse response, it is possible to produce frequency domain conversions of the response. Taking the ratio of the differential mode gain and the common mode gain over frequency will then provide the AC CMRR response, which can be evaluated for acceptability.

Part 2 Summary

Part 1 explained the use of differential signaling is becoming increasingly common in new data communication interfaces. Differential signaling is being used in gigabit serial data links because of a number of performance advantages. Application requirements for increasingly faster data rates mean that physical interconnect design limits are being pushed and that jitter and loss effects must be carefully managed. Pushing design limits also requires that designs be tested to verify simulated performance, to check standards compliance, and to debug problems.

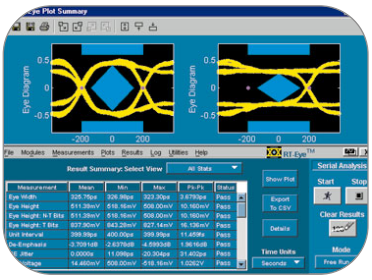
Part 2 reviewed differential measurement issues that need to be understood for effective differential signal testing. High-speed differential probe performance characteristics were examined so that probe limitations and their effect on measurement fidelity might be understood. Techniques for reliable probe attachment were also reviewed, since probe connections are such an important part of probe performance. Finally, differential measurements in a 50 Ω signaling environment were discussed using both pseudo-differential methods and a new differential probe architecture. As probing technology evolves for the most challenging applications, Tektronix is committed to providing the high performance measurement tools needed to support the testing of high-speed differential signals.

▶ **P7350SMA – 5.0 GHz Differential Probe with SMA Input.** The P7350 SMA provides a more efficient measurement solution for the new high-speed serial data standards. By integrating a dual 50 Ω termination network and a differential amplifier in the probe head, the P7350SMA provides the ability to measure a differential signal pair on each channel of a multiple channel oscilloscope. Tektronix is proving its expertise in differential probing.

▶ **P7350 – High-speed Differential Probe.** The P7350 improves usability with variable spacing and solder down capability, and a small form factor for ease of use on densely packed circuit boards. It employs the patented TekConnect™ Interface, which preserves signal integrity to 10 GHz and beyond to meet present and future bandwidth needs.

▶ **TDS8000B – Digital Sampling Oscilloscopes.** With excellent measurement repeatability, exceptional vertical resolution and fast waveform acquisition and display update rates, the TDS8000B is a powerful measurement tool for semiconductor testing, TDR characterization of circuit boards, IC packages and cables and high-speed digital communications.

▶ **TDS6000 – 6 GHz Digital Storage Oscilloscope.** With its ability to support single shot acquisition to 6 GHz, the TDS6000 Series is the first oscilloscope with multiple-channel acquisition at such speeds allowing you to accurately capture transients and fast signal edges that affect your digital system's performance.



▶ **TDSRT-Eye™ –** TDSRT-EYE Serial Data Compliance and Analysis Software takes the guesswork out of compliance testing by providing a complete solution from probe tip to compliance report for emerging copper serial data standards.

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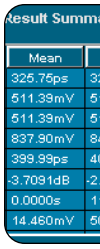

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